dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 family devices that you have received conform functionally to the current Device Data Sheet (DS75018**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on Page 8, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ06GS001/101A/102A/202A and dsPIC33FJ09GS302 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
dsPIC33FJ06GS001	0x4900	0x3001
dsPIC33FJ06GS101A	0x4901	
dsPIC33FJ06GS102A	0x4904	
dsPIC33FJ06GS202A	0x4905	
dsPIC33FJ09GS302	0x4906	

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70659) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Revisions[1]
				A1
CPU	Instruction Set	1.	When using the `div.sd` instruction, the overflow bit is not getting set when an overflow occurs.	X
CPU	Interrupt Disable	2.	When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X
PWM	PWM Module Enable	3.	A glitch may be observed on the PWM pins when the PWM module is enabled after assignment of pin ownership to the PWM module.	X
PWM	Master Time Base Mode	4.	In Master Time Base mode, writing to the Period register, and any other timing parameter of the PWM module, will cause the update of the other timing parameter to take effect, one PWM cycle after the period update is effective.	X
PWM	PWM Module Enable	5.	If the PWM Clock Divider Select Register, PTCON2, is not equal to zero, the PWM module may or may not initialize from an override state	X
CPU	Sleep Mode	6.	When the VREGS bit (RCON<8>) is set to a logic '0', and the device enters into Sleep mode, the device cannot wake-up.	X
SPI	Frame Sync	7.	When the SPI module is configured in Framed Master mode and the Frame Sync Pulse Edge Select bit (FRMDLY) is set to '1', transmitting a word and then buffering another word in the SPIxBUF register, before the transmission has completed, results in an incomplete transmission of the first data word.	X
SPI	Frame Sync	8.	When is in SPI Slave mode, with the Frame Sync pulse set as an input, FRMDLY must be set to '0'.	X
UART	TX Interrupt	9.	A Transmit (TX) Interrupt may occur before the data transmission is complete.	X
UART	UARTEN	10.	The Transmitter Write Pointer does not get cleared when the UART is disabled (UARTEN = 0); it requires TXEN to be set in order to clear the Write Pointer.	X
Comparator	Comparator Output	11.	A glitch may occur on the comparator output when the comparator module is enabled (CMPON = 1).	X
Comparator	External Reference	12.	Comparator and DACOUT do not function when EXTREF is enabled and EXTREF input voltage is less than 1.6V.	X
PWM	Immediate Update	13.	When the Immediate Update Enable bit (IUE = 1) is set, it is possible for the dead time to not be asserted during a PDCx register update.	X
PWM	Center-Aligned Mode	14.	PWMxH is asserted for 100% of the PWM period in Complementary mode under certain circumstances.	X
Comparator	Filter	15.	The digital filter does not function per design specification.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always become set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A1							
X							

2. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for '`n`'.

Affected Silicon Revisions

A1							
X							

3. Module: PWM

The PENH and PENL bits in the IOCONx register are used to assign ownership of the pins to either the PWM module or the GPIO module. The correct procedure to configure the PWM module is to first assign pin ownership to the PWM module and then enabling it using the PTEN bit in the PTCON register.

If the PWM module is enabled using the above sequence, then a glitch may be observed on the PWM pins before actual switching of the PWM outputs begins. This glitch may cause momentary turn ON of power MOSFETs that are driven by the PWM pins and may cause damage to the application hardware.

Work around

Perform the following steps to avoid any glitches from appearing on the PWM outputs at the time of enabling:

1. Configure the respective PWM pins to digital inputs using the TRISx registers. This step will put the PWM pins in a high-impedance state. The PWM outputs must be maintained in a safe state by using pull-up or pull-down resistors.
2. Assign pin ownership to the GPIO module by configuring the PENH bit (IOCONx<15>) = 0 and the PENL bit (IOCONx<14>) = 0.
3. Specify the PWM override state to the desired safe state for the PWM pins using the OVRDAT<1:0> bit field in the IOCONx register.
4. Override the PWM outputs by setting the OVRENH bit (IOCONx<9>) = 1 and the OVRENL bit (IOCONx<8>) = 1.
5. Enable the PWM module by setting the PTEN bit (PTCON<15>) = 1.
6. Remove the PWM overrides by making the OVRENH bit (IOCONx<9>) = 0 and the OVRENL bit (IOCONx<8>) = 0.
7. Ensure a delay of at least one full PWM cycle.
8. Assign pin ownership to the PWM module by setting the PENH bit (IOCONx<15>) = 1 and the PENL bit (IOCONx<14>) = 1.

The code in Example 1 illustrates the use of this work around.

Affected Silicon Revisions

A1							
X							

EXAMPLE 1: CONFIGURE PWM MODULE TO PREVENT GLITCHES ON PWM1H AND PWM1L PINS AT THE TIME OF ENABLING

```
TRISAbits.TRISA4 = 1;      // Configure PWM1H/RA4 as digital input
                           // Ensure output is in safe state using pull-up or pull-down resistors
TRISAbits.TRISA3 = 1;      // Configure PWM1L/RA3 as digital input
                           // Ensure output is in safe state using pull-up or pull-down resistors

IOCON1bits.PENH = 0;       // Assign pin ownership of PWM1H/RA4 to GPIO module
IOCON1bits.PENL = 0;       // Assign pin ownership of PWM1L/RA3 to GPIO module

IOCON1bits.OVRDAT = 0;     // Configure PWM outputs override state to the desired safe state

IOCON1bits.OVRENH = 1;     // Override PWM1H output
IOCON1bits.OVRENL = 1;     // Override PWM1L output

PTCONbits.PTEN = 1;        // Enable PWM module

IOCON1bits.OVRENH = 0;     // Remove override for PWM1H output
IOCON1bits.OVRENL = 0;     // Remove override for PWM1L output

Delay(x);                  // Introduce a delay greater than one full PWM cycle

IOCON1bits.PENH = 1;       // Assign pin ownership of PWM1H/RA4 to PWM module
IOCON1bits.PENL = 1;       // Assign pin ownership of PWM1L/RA3 to PWM module
```

4. Module: PWM

The high-speed PWM module can operate with variable period, duty cycle, dead-time and phase values. The master period and other timing parameters can be updated in the same PWM cycle. With immediate updates disabled, the new values should take effect at the start of the next PWM cycle.

As a result of this erratum, the updated master period takes effect on the next PWM cycle, while the update of the additional timing parameter is delayed by one PWM cycle. The parameters affected by this erratum are as follows:

Master Period Registers: Update effective on the next PWM cycle:

- PTPER: If PWMCONx<MTBS> = 0
- STPER: If PWMCONx<MTBS> = 1

Additional PWM Timing Parameters: Update effective one PWM cycle after master period update:

- Duty Cycle: PDCx, SDCx and MDC registers
- Phase: PHASEx or SPHASEx registers
- Dead Time: DTRx and ALTDTRx registers and dead-time compensation signals
- Clearing of current-limit and Fault conditions, and application of External Period Reset signal

Work around

If the application requires the master period and other parameters to be updated at the same time, enable both immediate updates:

- PTCON<EIPU> = 1 to enable immediate period updates
- PWMCONx<IUE> = 1 to enable immediate updates of additional parameters listed above

Enabling immediate updates will allow updates to the master period and the other parameter to take effect immediately after writing to the respective registers.

Affected Silicon Revisions

A1							
X							

5. Module: PWM

If the PWM Clock Divider Select register (PTCON2) is not equal to zero, the PWM module may or may not initialize from an override state, even when the Override Enable bits are set (OVRENH = 1 or OVRENL = 1).

Work around

When configuring the Override Enable bits, OVRENH and OVRENL (IOCONx<9,8>), set these bits implicitly using word format; do not set them explicity using bit format.

That is, use this format:

```
IOCON1 = IOCON1 & 0xFCFF
```

and not this format:

```
IOCON1bits.OVRENH = 1
```

Affected Silicon Revisions

A1							
X							

6. Module: CPU

When the VREGS bit (RCON<8>) is set to a logic '0' and the device enters Sleep mode, the device cannot wake up.

Work around

Ensure that the VREGS bit (RCON<8>) is set to a logic '1' for device Sleep mode operation.

Affected Silicon Revisions

A1							
X							

7. Module: SPI

When the SPI module is configured in Framed Master mode and the Frame Sync Pulse Edge Select bit (FRMDLY) is set to '1', transmitting a word and then buffering another word in the SPIxBUF register, before the transmission has completed, results in an incomplete transmission of the first data word. Only the first 15 bits from the first data word are transmitted, followed by the Sync Pulse and the complete second word.

Work around

Between the two back-to-back SPI operations, add a delay to ensure that the first word is fully transmitted before the second word is written to the SPIxBUF register, as shown in Example 2.

EXAMPLE 2:

```
SPI1BUF = 0x0001;

while (SPI1STATbits.SPITBF);

    asm("REPEAT #50");.
    asm("NOP");

// The number of NOPs depends on the SPI
// clock prescalers

SPI1BUF = 0x0002;
```

Affected Silicon Revisions

A1							
X							

8. Module: SPI

When in SPI Slave mode (SPIxCON1<MSTEN> = 0) and using the Frame Sync Pulse output feature (SPIxCON2<FRMEN> = 1) in Slave mode (SPIxCON2<SPIFSD> = 0), the Frame Sync Pulse Edge Select bit must be set to '0' (SPIxCON2 <FRMDLY> = 0).

Work around

There is no work around. The Frame Sync Pulse Edge Select bit cannot be set to produce a Frame Sync Pulse that coincides with the first bit clock.

Affected Silicon Revisions

A1							
X							

9. Module: UART

When using UTXISEL<1:0> = 01 (interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) Interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occur only when all transmit operations are complete, hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A1							
X							

10. Module: UART

The Transmitter Write Pointer does not get cleared when the UART module is disabled (UARTEN = 0), and it requires the TXEN bit to be set in order to clear the Write Pointer.

Work around

Do not load data into the TX FIFO (register) before setting the TXEN bit.

Affected Silicon Revisions

A1							
X							

11. Module: Comparator

When the Comparator module is enabled (CMPON = 1), the output of the comparator is set high for approximately 300 ns, regardless of the comparator input signal level.

Work around

Allow at least 1 µs after the Comparator module is enabled (CMPON = 1) to initiate any comparator driven interrupts or Faults.

Affected Silicon Revisions

A1							
X							

12. Module: Comparator

The comparator and DAC modules do not function when both of the following are true:

- the External Voltage Reference is selected (EXTREF = 1), and
- the external voltage reference is less than 1.6V.

Work around

Use the INTREF or AVDD/2 references, whenever possible.

If the External Voltage Reference must be used, be aware that the published specifications for EXTREF define an input voltage range of 0V minimum and (AVDD – 1.6)V maximum. For the affected silicon revisions, the operational input voltage limits of EXTREF are 1.6V minimum and (AVDD – 0.6)V maximum.

Affected Silicon Revisions

A1							
X							

13. Module: PWM

The PWM generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- the PWM generator is configured to operate in Complementary mode with independent time base or master time base.
- immediate update is enabled
- the value in the PDCx register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

Work around

Disable the Immediate Update Enable bit (IUE).

Affected Silicon Revisions

A1							
X							

14. Module: PWM

In Center-Aligned Complementary mode with independent time base, the PWM generator may assert the PWMxH output for 100% of the duty cycle. This has been observed when the value in its PDCx register is less than one-half the value in its ALTDTRx register.

Work around

Include a software routine to check that the duty cycle value written to the PDCx register is always at least one-half of the value in ALTDTRx. Example 3 shows one way of doing this, with PDCtemp representing the value to be written to the PDCx register.

EXAMPLE 3:

```
    Altdtr_by2 = ALTDTRx / 2;
if (PDCtemp < Altdtr_by2)
{
        PDCx = Altdtr_by2;
}
else
{
        PDCx = PDCtemp;
}
```

Affected Silicon Revisions

A1							
X							

15. Module: Comparator

The Digital Filter does not function per design specification. When the FLTREN bit (CMPCON<10>) is enabled, it will generate a delay of approximately three cycles of the selected clock source. This results in unwanted comparator latency delay before changing the state of the comparator output and any of the interrupts driven by it.

Work around

The FLTREN bit (CMPCON <10>) should be reset to '0'.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS75018**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Characteristics

The Min and Typ values in Table 25-42 have been corrected. The correct values are shown in bold below:

TABLE 25-42: DAC MODULE SPECIFICATIONS

AC and DC CHARACTERISTICS(2)			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Comments
DA01	EXTREF	External Voltage Reference(1)	0	—	AVDD – 1.6	V	
DA08	INTREF	Internal Voltage Reference(1)	1.15	1.25	1.35	V	
DA02	CVRES	Resolution	10			Bits	
DA03	INL	Integral Nonlinearity Error	-7	-1	+7	LSB	AVDD = 3.3V, DACREF = (AVDD/2)V
DA04	DNL	Differential Nonlinearity Error	-5	-0.5	+5	LSB	
DA05	EOFF	Offset Error	**-0.8**	**0.4**	2.6	%	
DA06	EG	Gain Error	**-1.8**	**0.4**	5.2	%	
DA07	TSET	Settling Time**(1)**	711	1551	2100	ns	Measured when range = 1 (high range) and the CMREF<9:0> bits transition from 0x1FF to 0x300.

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: Overall functional device operation at VBORMIN < VDD < VDDMIN is tested but not characterized. All device analog modules, such as the ADC, etc., will function but with degraded performance below VDDMIN. Refer to Parameter BO10 in Table 25-11 for BOR values.

2. Module: Oscillator Configuration

Bit CF in Register 8-1 was stated as R/C-0. The correct definition is R/W-0. The (read/clear by application) text has also been removed from the CF bit description on Page 127.

3. Module: Oscillator Configuration

The values describing the range of tenability of the internal oscillator in Register 8-4 have been corrected. The correct values are shown in bold below:

REGISTER 8-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER(2)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN<5:0>(1)					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0 TUN<5:0>: FRC Oscillator Tuning bits(1)

011111 = Center frequency + **1.45% (7.478 MHz)**
011110 = Center frequency + 1.**40% (7.4743 MHz)**
•
•
•
000001 = Center frequency + **0.047% (7.3734 MHz)**
000000 = Center frequency **(7.37 MHz)**
111111 = Center frequency **-0.047% (7.366 MHz)**
•
•
•
100001 = Center frequency **-1.453% (7.263 MHz)**
100000 = Center frequency **-1.5% (7.26 MHz)**

Note 1: OSCTUN functionality has been provided to help customers compensate for temperature effects on the FRC frequency over a wide range of temperatures. The tuning step-size is an approximation and is neither characterized nor tested.

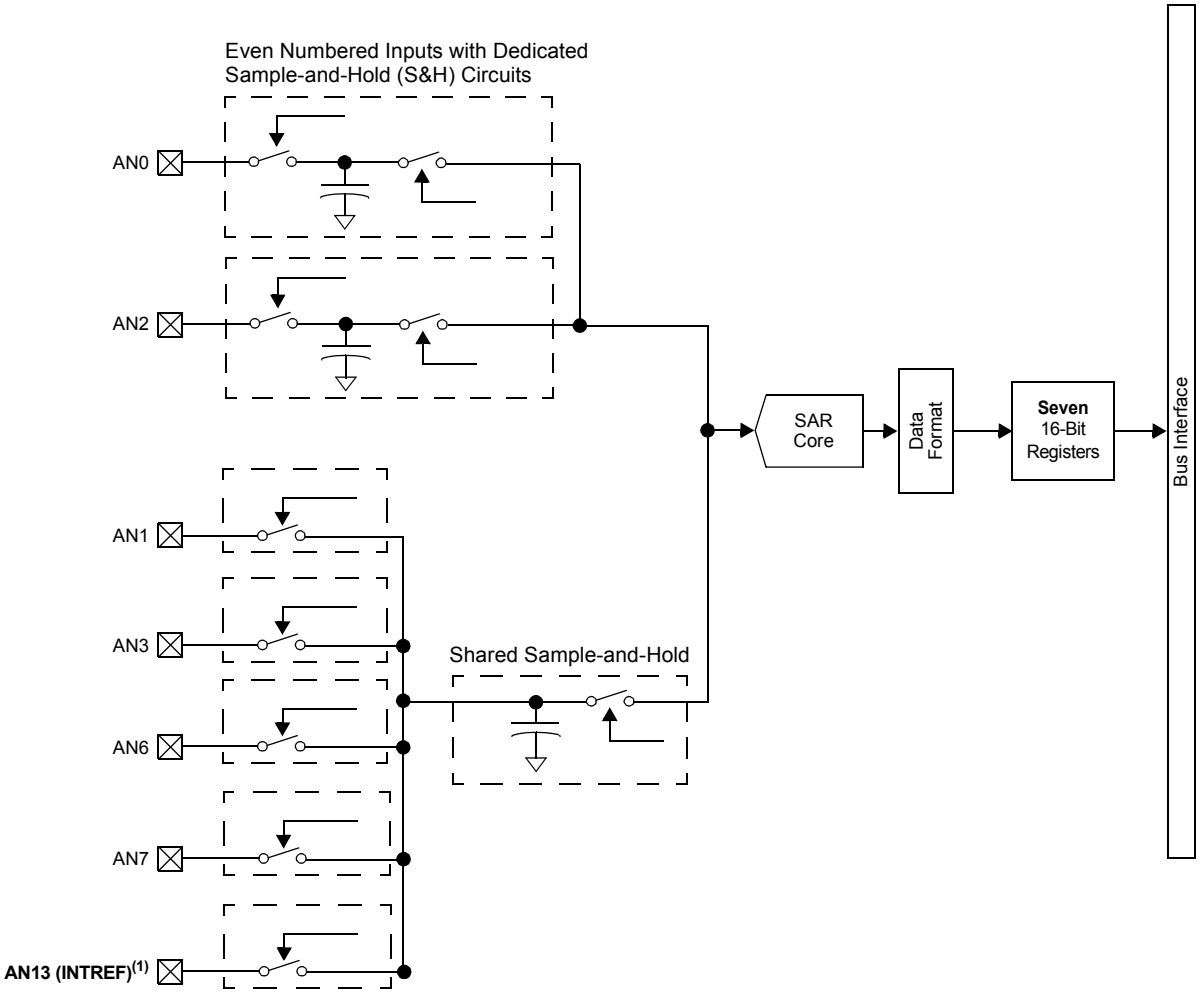
2: This register is reset only on a Power-on Reset (POR).

4. Module: High-Speed, 10-Bit Analog-to-Digital Converter (ADC)

In Figure 19-2 and Figure 19-3, AN13 has been added and the number of output registers has been changed from eight to seven.

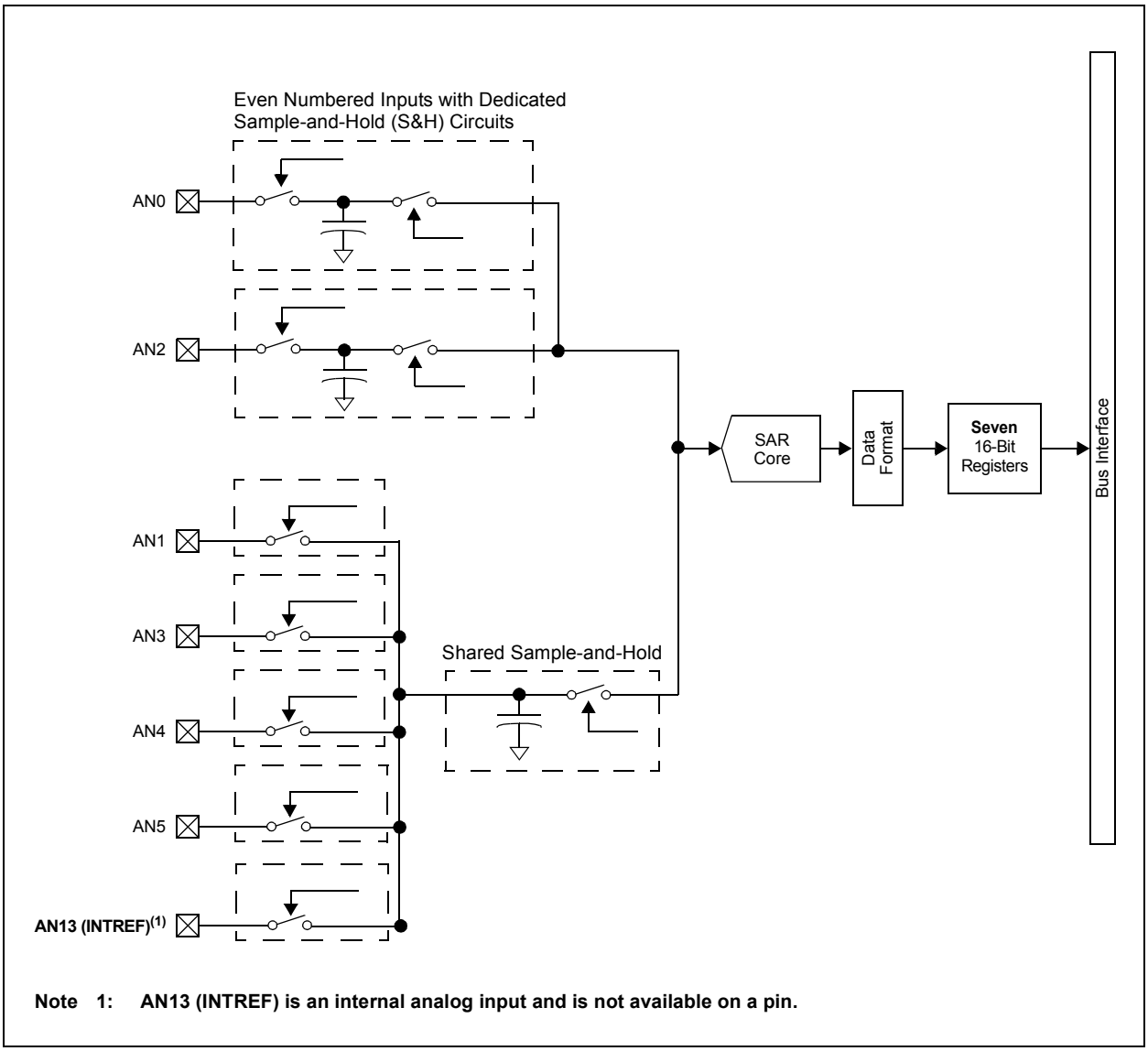
In Figure 19-5, the number of output registers has been changed from eight to ten. The changes are shown in bold below:

FIGURE 19-2: ADC BLOCK DIAGRAM FOR THE dsPIC33FJ06GS101A DEVICE



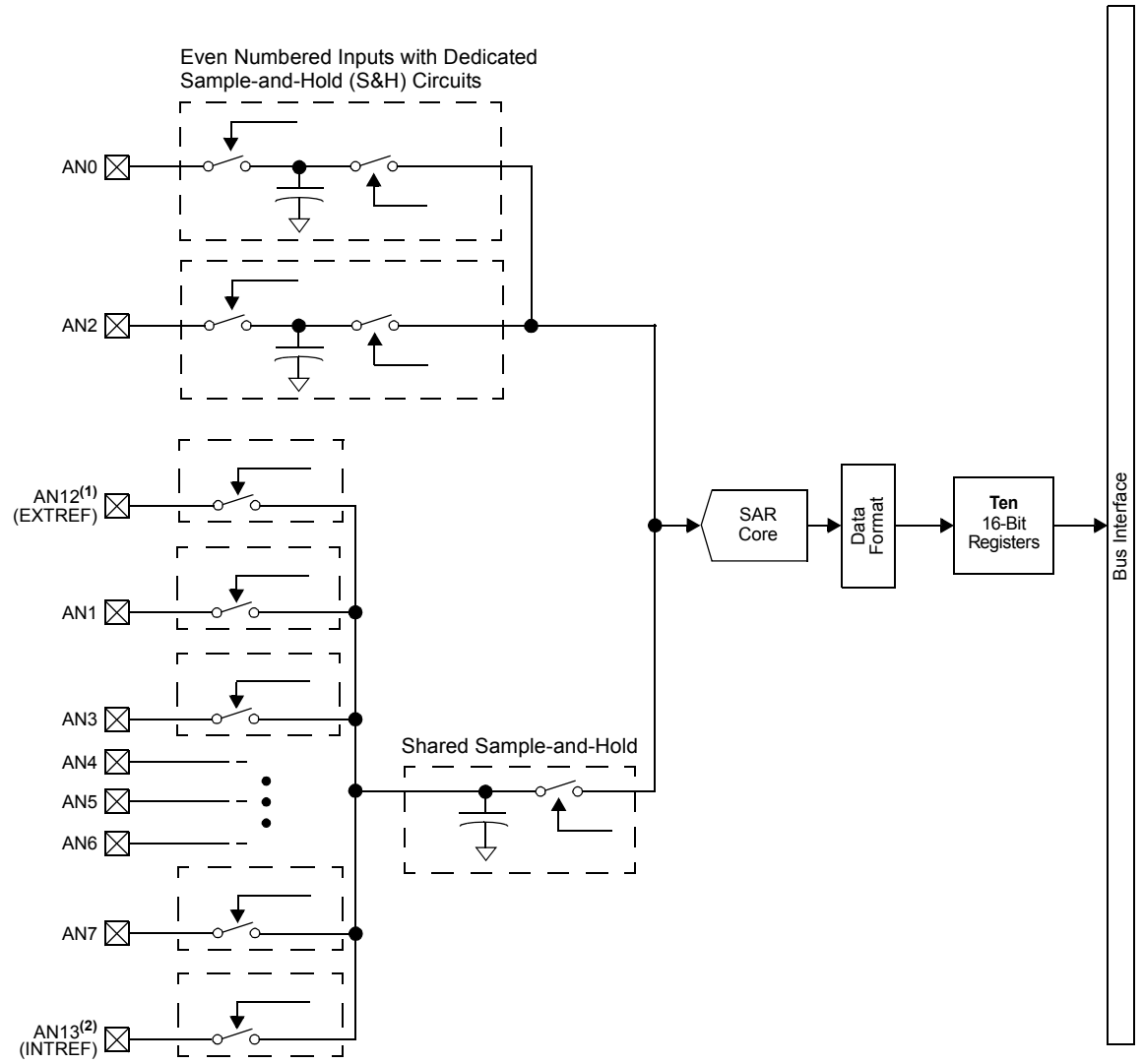
Note 1: AN13 (INTREF) is an internal analog input and is not available on a pin.

FIGURE 19-3: ADC BLOCK DIAGRAM FOR THE dsPIC33FJ06GS102A DEVICE



Note 1: AN13 (INTREF) is an internal analog input and is not available on a pin.

FIGURE 19-5: ADC BLOCK DIAGRAM FOR THE dsPIC33FJ09GS302 DEVICE



Note 1: To measure the voltage at AN12 (EXTREF), an analog comparator must be enabled and EXTREF must be selected as the comparator reference.

2: AN13 (INTREF) is an internal analog input and is not available on a pin.

APPENDIX A: REVISION HISTORY

Rev A Document (3/2012)

Initial release of this document; issued for revision A0 silicon.

Included silicon issues 1 (CPU), 2 (CPU), 3 (GPIO), 4 (PGEC2/PGED2 Programming Pins (dsPIC33FJ06GS001/101A/102A Devices Only)), 5-9 (PWM), 10 (Sleep Mode), 11 (Sleep Mode), 12 (SPI), 13 (SPI), 14 (UART), 15 (UART), 16 (Comparator), and 17 (Comparator).

Rev B Document (7/2012)

Removes silicon revision A0 and all issues, as this revision was never released.

Adds silicon revision A1 in its place. Includes new silicon issues 1-2 (CPU), 3-5 (PWM), 6 (CPU), 7-8 (SPI), 9-10 (UART) and 11-12 (Comparator).

Rev C Document 1/2013

Adds silicon revisions 13-14 (PWM).

Rev D Document 2/2013

Adds silicon issue 15 (Comparator). Adds data sheet clarifications 1 (Electrical Characteristics), 2-3 (Oscillator Configuration) and 4 (High-Speed, 10-Bit Analog-to-Digital Converter (ADC)).

NOTES:

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Printed on recycled paper.

ISBN: 978-1-62077-003-0

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China - Xian
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China - Xiamen
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China - Zhuhai
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India - Pune
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Japan - Osaka
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Japan - Tokyo
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Korea - Daegu
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Korea - Seoul
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Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
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Malaysia - Penang
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Philippines - Manila
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