



STL42N65M5

N-channel 650 V, 0.070 Ω , 34 A MDmesh™ V Power MOSFET in PowerFLAT™ 8x8 HV package

Datasheet — preliminary data

Features

Order code	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STL42N65M5	710 V	< 0.079 Ω	34 A ⁽¹⁾

1. The value is rated according to R_{thj-case}

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

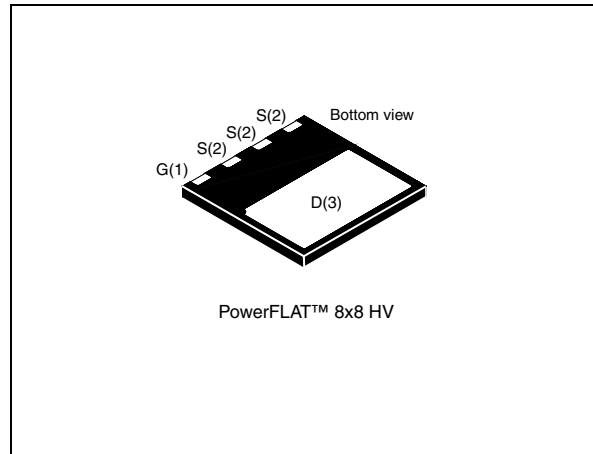


Figure 1. Internal schematic diagram

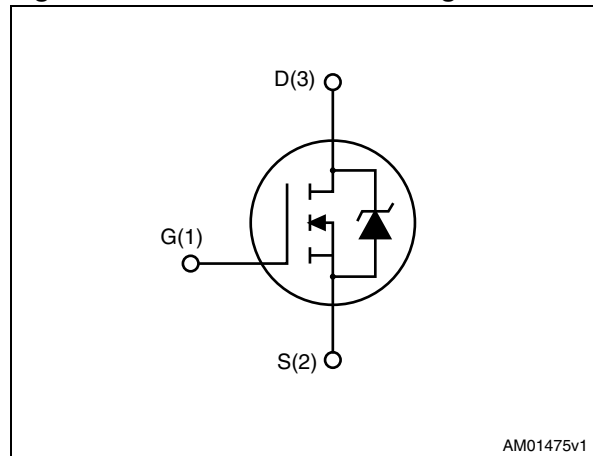


Table 1. Device summary

Order code	Marking	Package	Packaging
STL42N65M5	42N65M5	PowerFLAT™ 8x8 HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	34	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	22	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	136	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	4	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.5	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	3	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	208	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	11	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	950	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to $R_{thj-case}$.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of 1 inch^2 , 2oz Cu.
4. $I_{SD} \leq 34\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch^2 , 2oz Cu.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 16.5\text{ A}$		0.070	0.079	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	4650	-	μF
C_{oss}	Output capacitance			110		μF
C_{rss}	Reverse transfer capacitance			5.7		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0, V_{DS} = 0\text{ to }80\% V_{(BR)DSS}$	-	400	-	μF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related			285		μF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	1.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 16.5\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 3)	-	100	-	nC
Q_{gs}	Gate-source charge			26		nC
Q_{gd}	Gate-drain charge			38		nC

- $C_{o(er)}^{(1)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
- $C_{o(tr)}^{(2)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 400\text{ V}$, $I_D = 20\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 7)	-	TBD	-	ns
t_r	Rise time			TBD		ns
t_c	Cross time			TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		34	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				136	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 33\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 33\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 4)	-	400		ns
Q_{rr}	Reverse recovery charge			7		μC
I_{RRM}	Reverse recovery current			35		A
t_{rr}	Reverse recovery time	$I_{SD} = 33\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 4)	-	532		ns
Q_{rr}	Reverse recovery charge			10		μC
I_{RRM}	Reverse recovery current			38		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

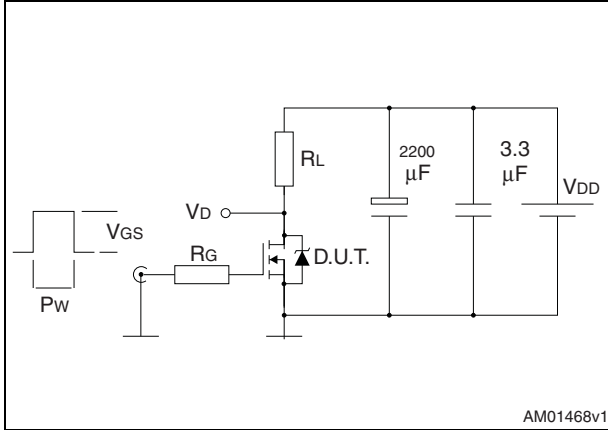


Figure 3. Gate charge test circuit

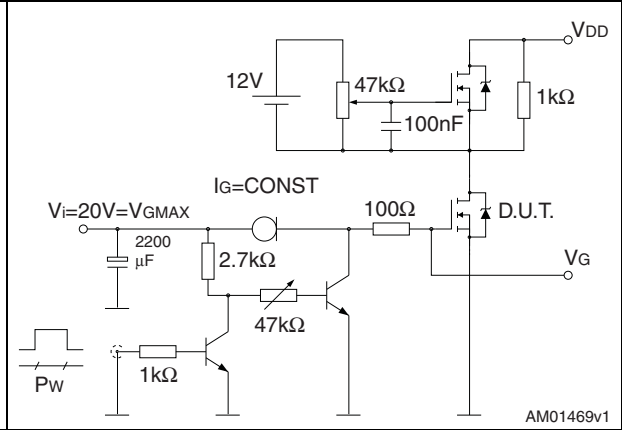


Figure 4. Test circuit for inductive load switching and diode recovery times

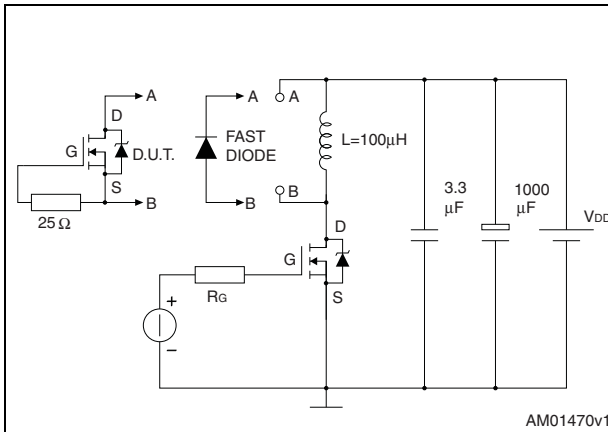


Figure 5. Unclamped inductive load test circuit

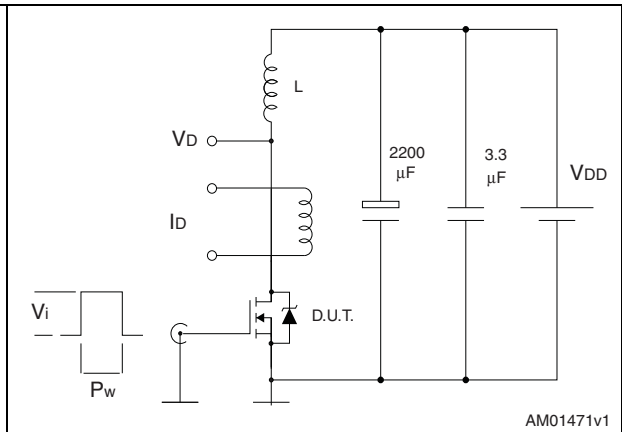


Figure 6. Unclamped inductive waveform

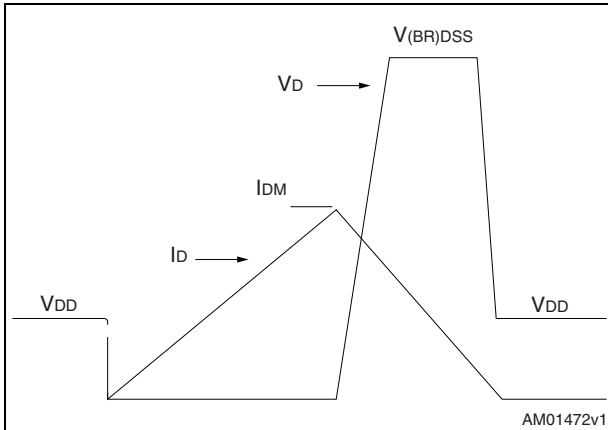
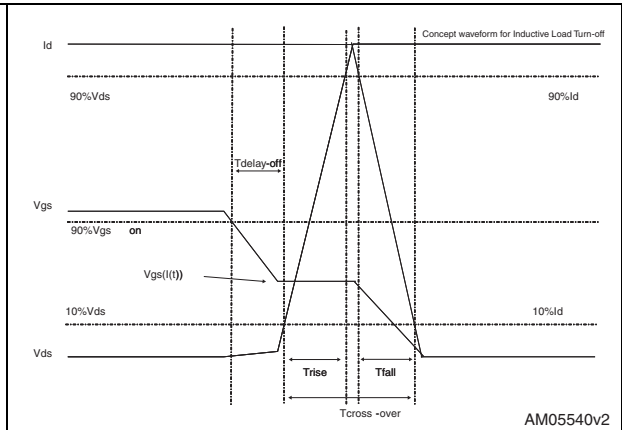


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

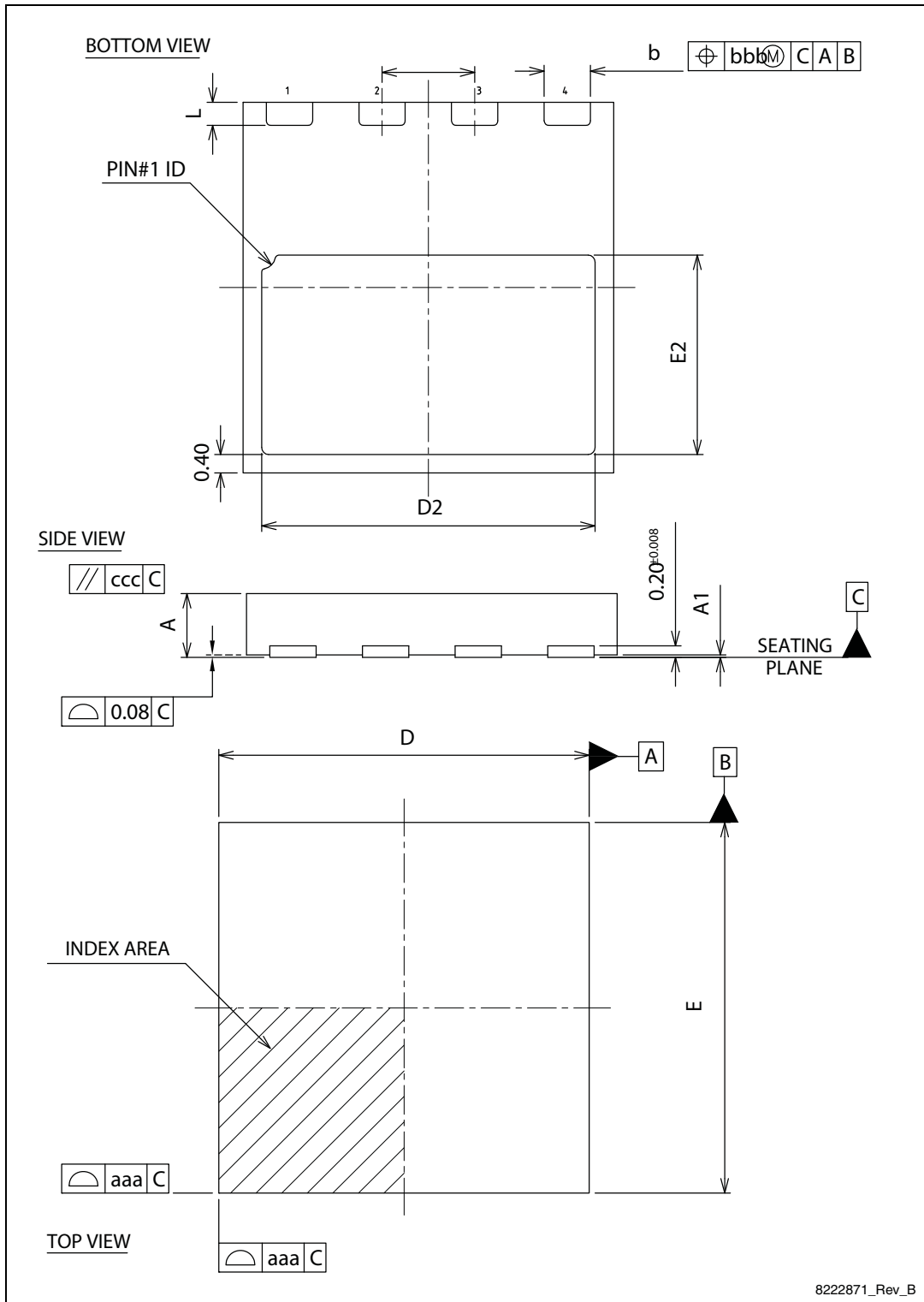
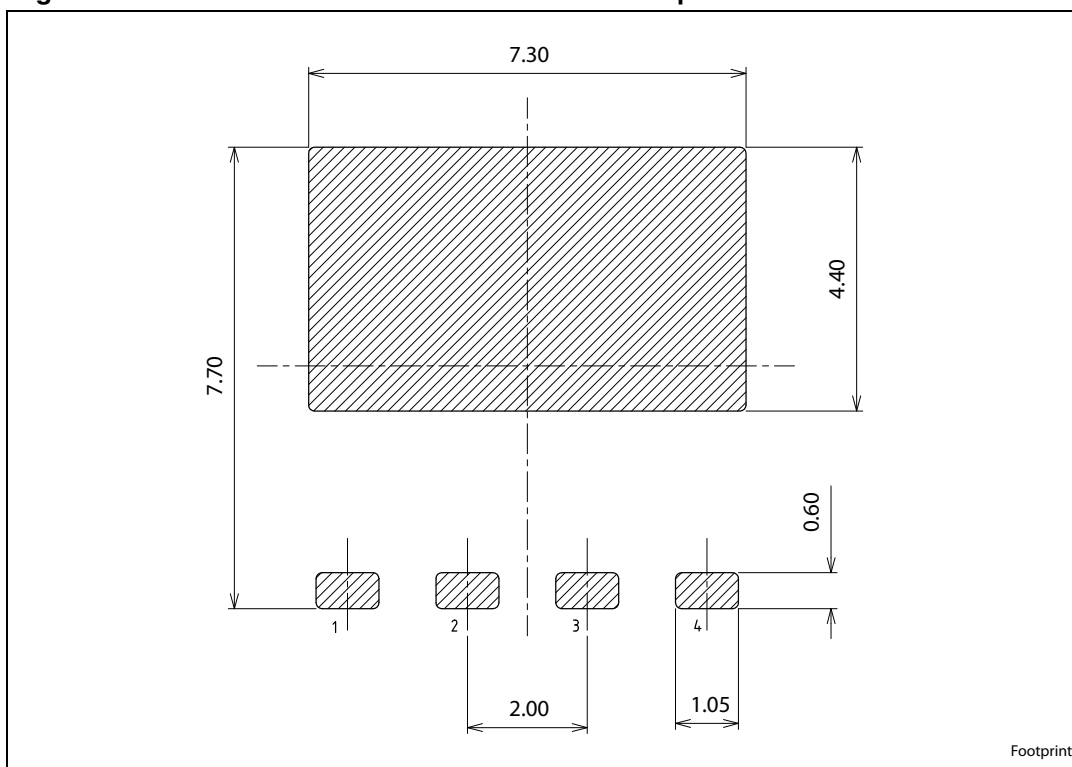


Figure 9. PowerFLAT™ 8x8 HV recommended footprint



5 Packaging mechanical data

Figure 10. PowerFLAT™ 8x8 HV tape

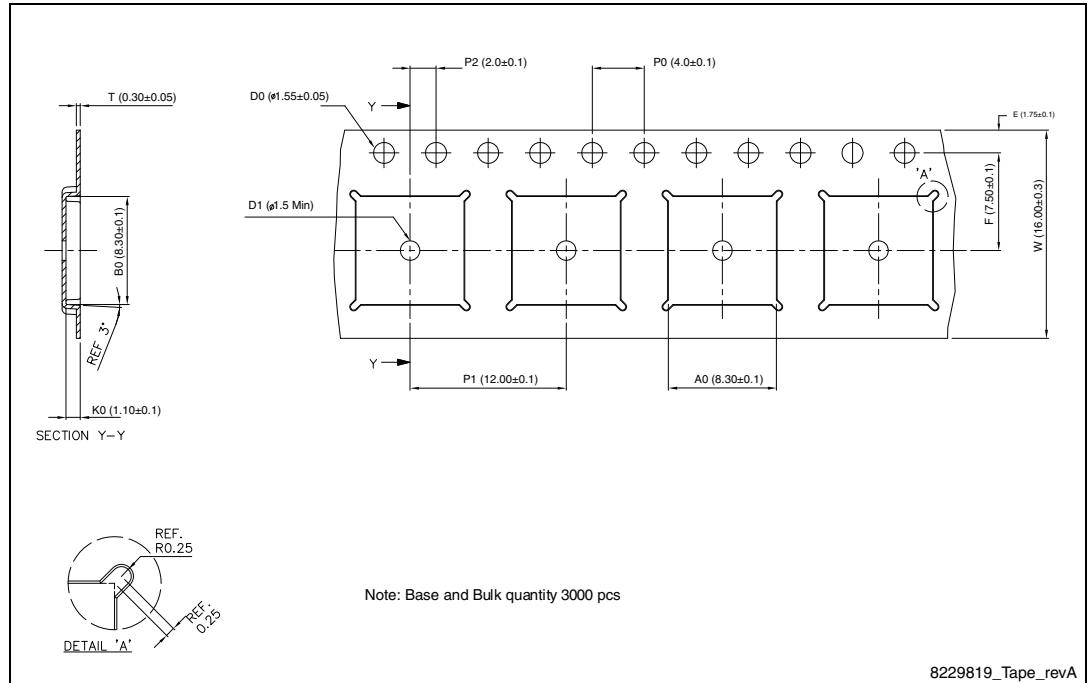
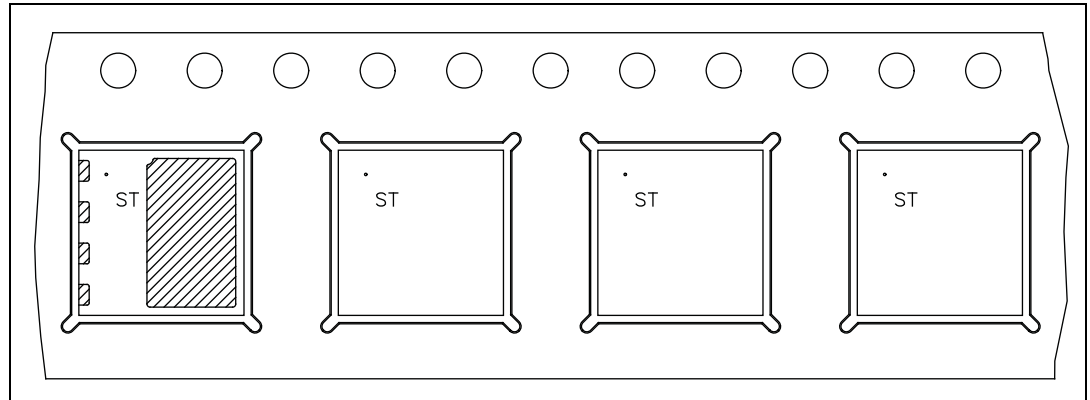


Figure 11. PowerFLAT™ 8x8 HV package orientation in carrier tape.



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
28-Apr-2010	1	First release.
27-Apr-2012	2	<i>Section 4: Package mechanical data</i> has been updated. Added new section: <i>Section 5: Packaging mechanical data</i> . Minor text changes.

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