

PHD96NQ03LT

N-channel TrenchMOS logic level FET

Rev. 06 — 15 March 2010

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge

1.3 Applications

- DC-to-DC convertors

1.4 Quick reference data

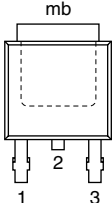
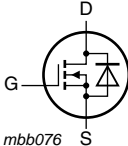
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ see Figure 1 and 3	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	115	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 50\text{ A};$ $V_{DS} = 15\text{ V}; T_j = 25\text{ °C};$ see Figure 11	-	8.4	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 9	-	4.2	4.95	m Ω
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A};$ $T_j = 25\text{ °C};$ see Figure 9 and 10	-	5.6	7.5	m Ω



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT428 (DPAK)</p>	 <p>mbb076</p>
2	D	drain [1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

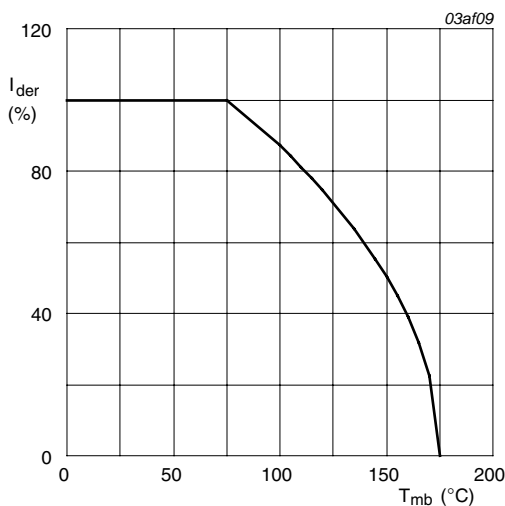
Type number	Package		Version
	Name	Description	
PHD96NQ03LT	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values

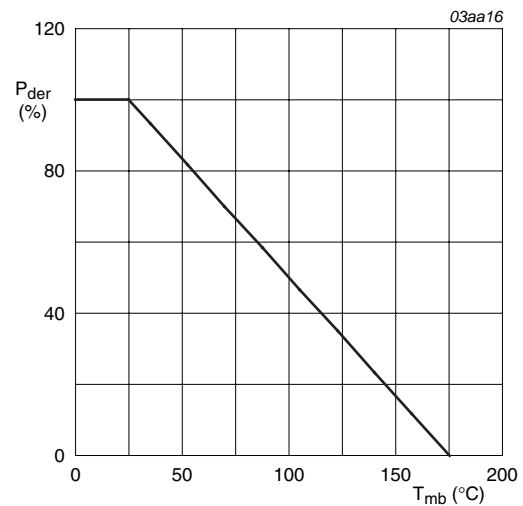
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	25	V
V _{DGR}	drain-gate voltage	T _j ≤ 175 °C; T _j ≥ 25 °C; R _{GS} = 20 kΩ	-	25	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 100 °C; see Figure 1 V _{GS} = 5 V; T _{mb} = 25 °C; see Figure 1 and 3	-	65 75	A
I _{DM}	peak drain current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C; see Figure 3	-	240	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	115	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	75	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	240	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 43 A; V _{sup} ≤ 15 V; R _{GS} = 50 Ω; t _p = 0.25 ms; unclamped	-	185	mJ
I _{DS(AL)S}	non-repetitive drain-source avalanche current	V _{GS} = 10 V; V _{sup} ≤ 15 V; R _{GS} = 50 Ω; T _{j(init)} = 25 °C; unclamped	-	75	A



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

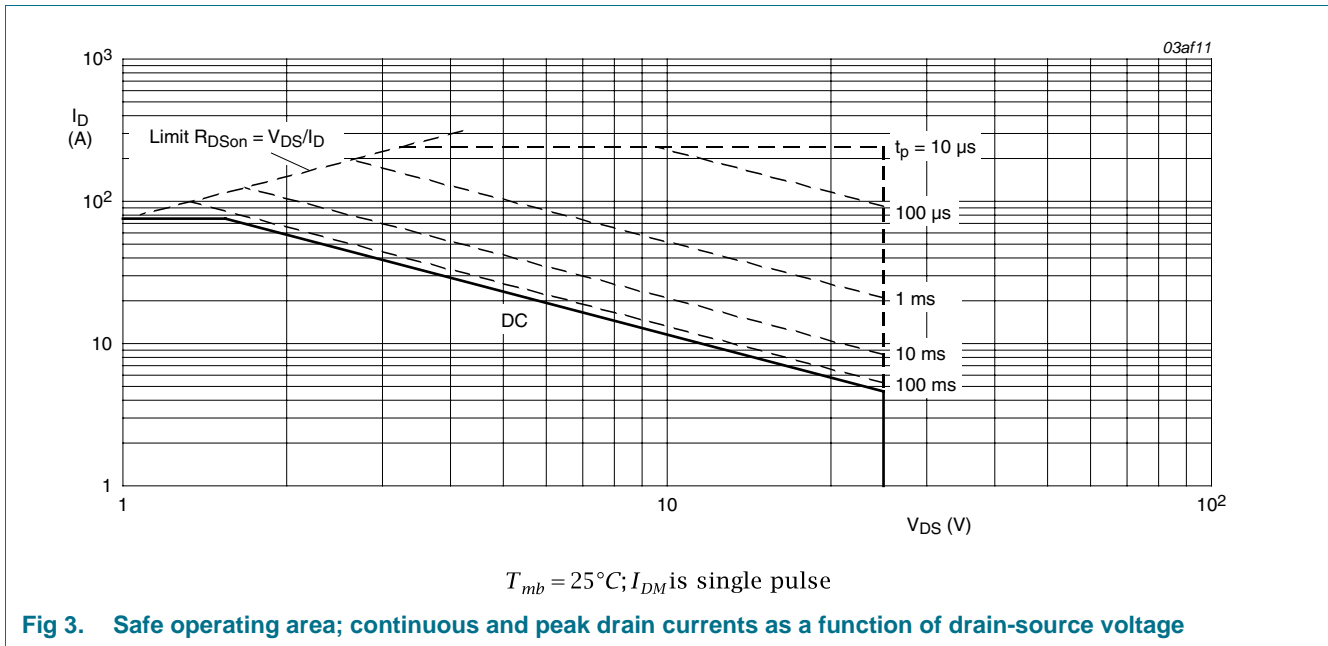


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; mounted on a printed-circuit board	-	75	-	K/W

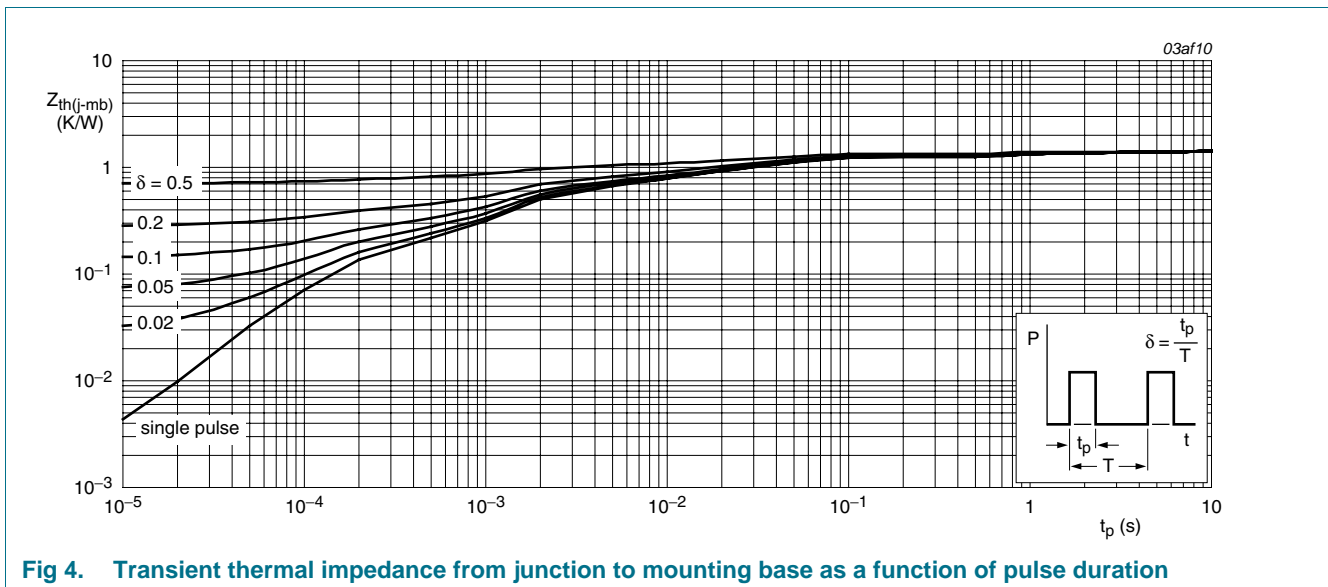
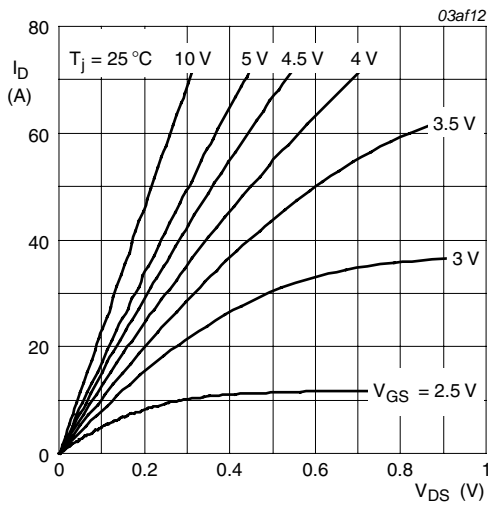


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

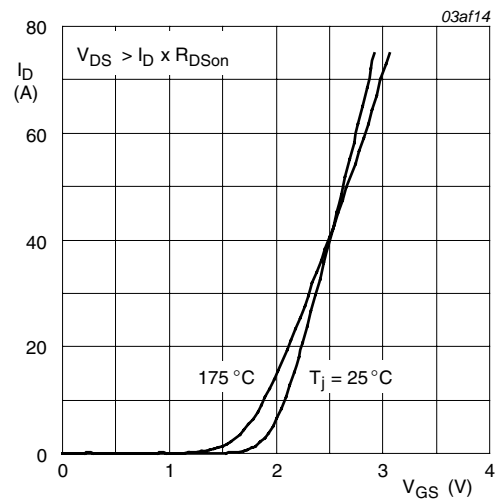
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	22	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 8	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 8	-	-	2.3	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 8	1	1.5	2	V
I_{DSS}	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	1	μA
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 9 and 10	-	10	13.5	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 9	-	4.2	4.95	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 9 and 10	-	5.6	7.5	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 5 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 11	-	26.7	-	nC
Q_{GS}	gate-source charge		-	8.5	-	nC
Q_{GD}	gate-drain charge		-	8.4	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 12	-	2200	-	pF
C_{oss}	output capacitance		-	725	-	pF
C_{rss}	reverse transfer capacitance		-	290	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 1.2 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 12.5 \text{ A}$	-	18	-	ns
t_r	rise time		-	70	-	ns
$t_{d(off)}$	turn-off delay time		-	75	-	ns
t_f	fall time		-	70	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 13	-	0.9	1.2	V
t_{rr}	reverse recovery time	$I_S = 10 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	43	-	ns
Q_r	recovered charge		-	40	-	nC



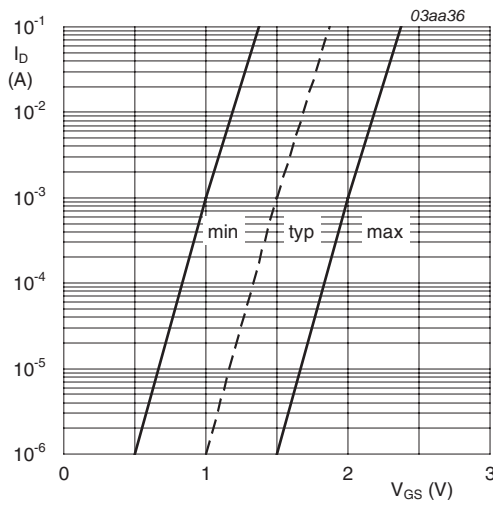
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



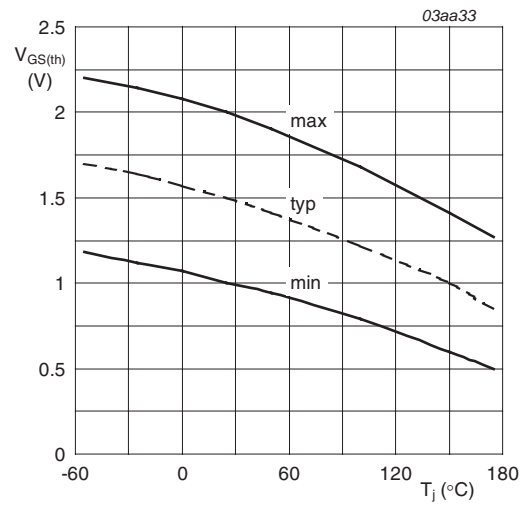
$T_j = 25^\circ\text{C}$ and $175^\circ\text{C}; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



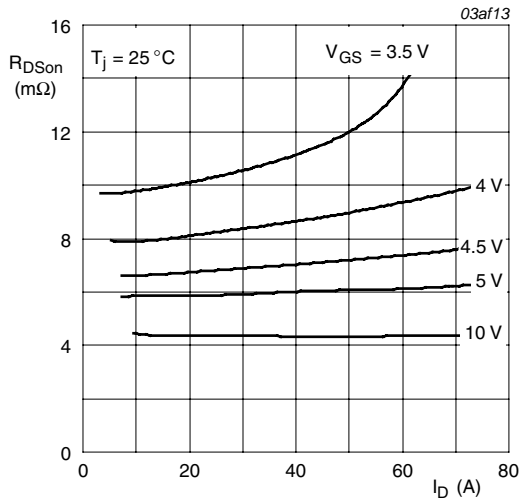
$T_j = 25^\circ\text{C}; V_{DS} = V_{GS}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



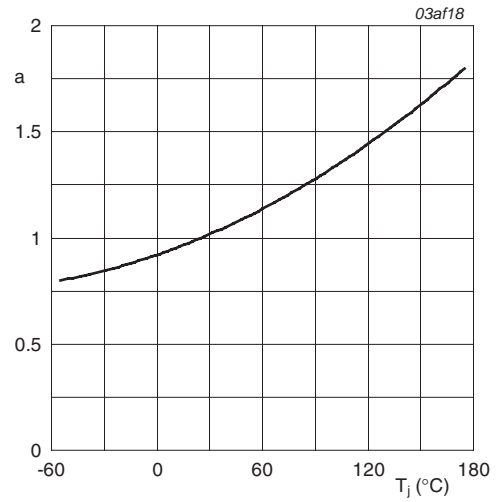
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



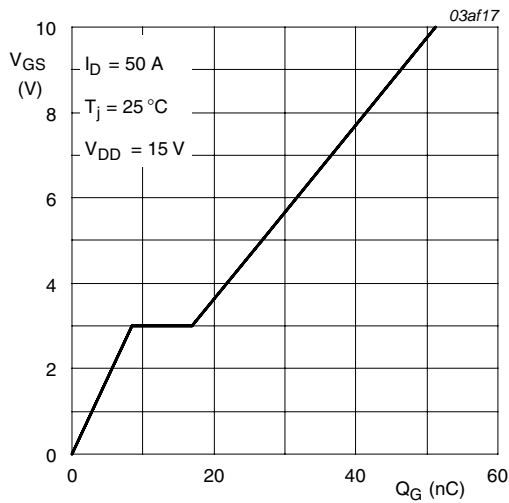
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



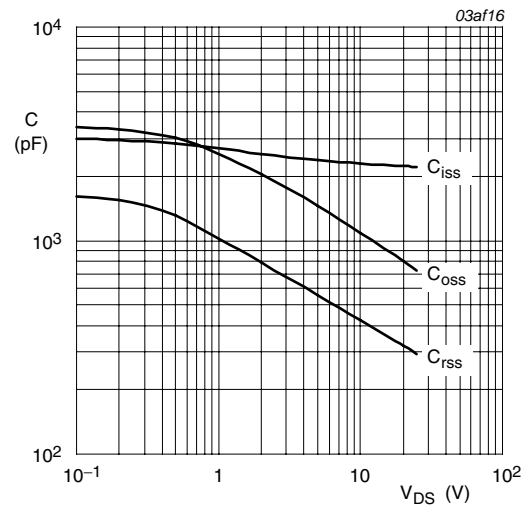
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



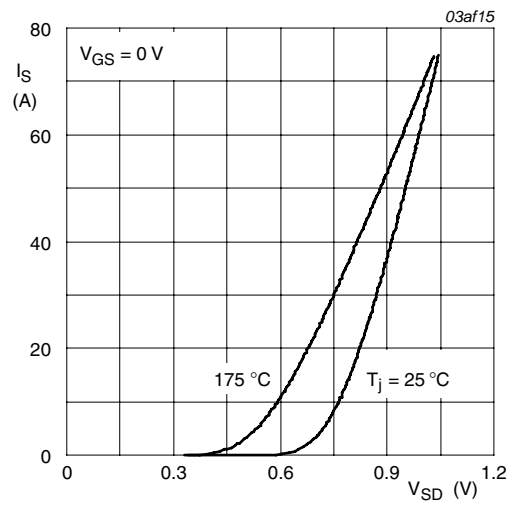
$I_D = 50\text{ A}; V_{DS} = 15\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ C$ and $175^\circ C; V_{GS} = 0V$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)

SOT428

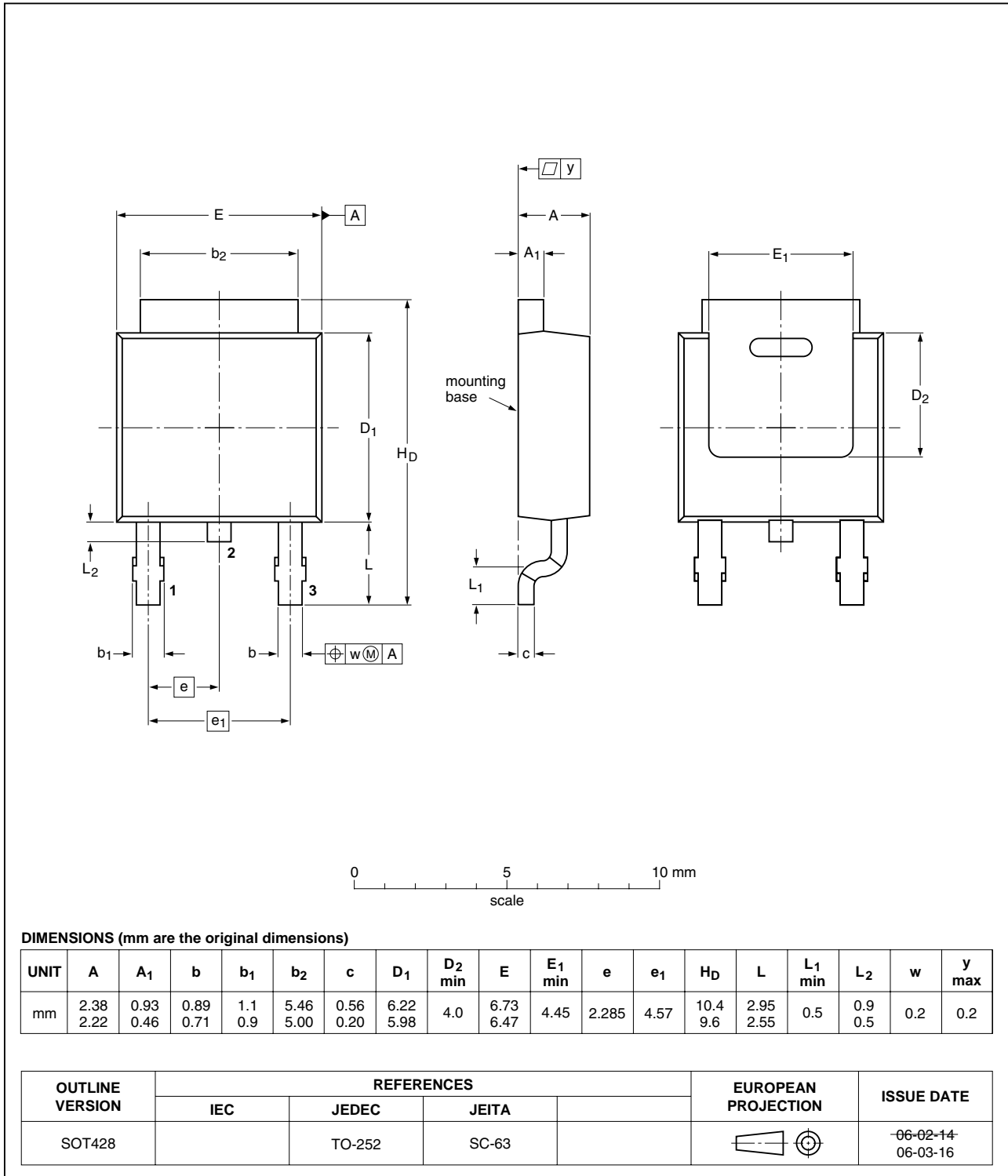


Fig 14. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD96NQ03LT_6	20100315	Product data sheet	-	PHP96NQ03LT-05
Modifications:				
			<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.	
PHP96NQ03LT-05 (9397 750 09666)	20020605	Product data	-	PHP96NQ03LT-04
PHP96NQ03LT-04	20020220	Product data	-	PHP96NQ03LT-03
PHP96NQ03LT-03	20011023	Product data	-	PHP96NQ03LT-02
PHP96NQ03LT-02	20011008	Product data	-	PHP96NQ03LT-01
PHP96NQ03LT-01	20010716	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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