PESD5V0S2BQA

Protection against high surge currents in ultra small DFN1010D-3 package

1 June 2016 **Product data sheet**

1. General description

Two bidirectional ElectroStatic Discharge (ESD) protection diodes designed to protect two signal lines from the damage caused by ESD and other transients.

The device is housed in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

2. Features and benefits

- Bidirectional ESD protection of two lines
- Ultra small SMD plastic package
- ESD protection up to 30 kV
- AEC-Q101 qualified
- IEC 61000-4-5 (surge): I_{PPM} = 14 A
- IEC 61000-4-5 (surge): I_{PPM} = 28 A combined lines
- Ultra low leakage current: I_{RM} = 1 nA

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics

4. Quick reference data

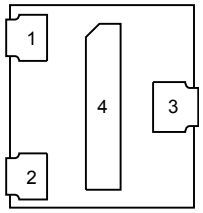
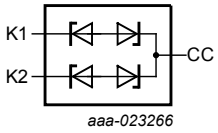
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; single line	[1]	-	35	45	pF

[1] Measured from pin 1 or 2 to pin 3.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode	 Transparent top view **DFN1010D-3 (SOT1215)**	
2	K2	cathode		
3	CC	common cathode		
4	CC	common cathode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0S2BQA	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5V0S2BQA	00 01 10

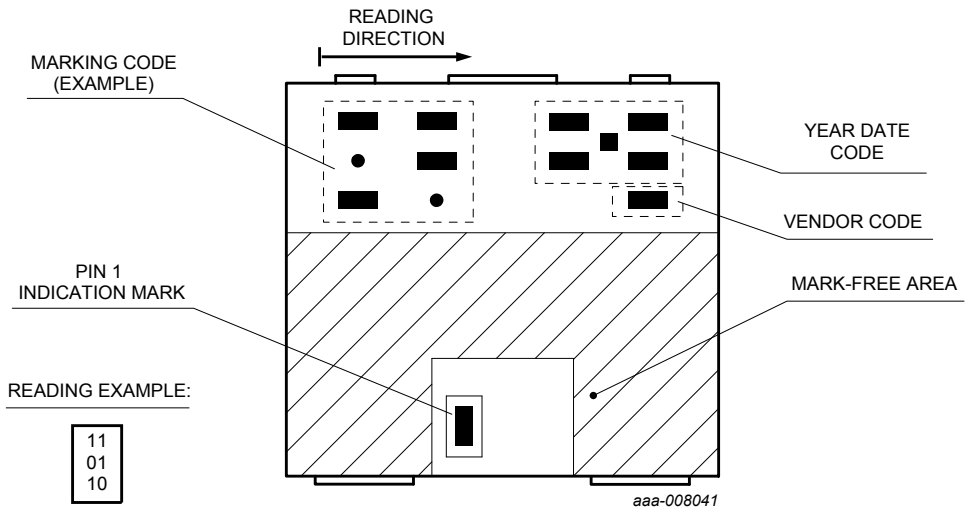


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	peak pulse current	t_p = 8/20 µs; single line	[1][2]	-	14	A
		t_p = 8/20 µs; combined lines	[1][3]	-	28	A
		t_p = 8/20 µs; average measured; single line	[1][2]	-	17.5	A
		t_p = 8/20 µs; average measured; combined lines	[1][3]	-	35	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	125	°C
T_{stg}	storage temperature			-65	150	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	contact discharge	[4][2]	-	30	kV
		air discharge	[4][2]	-	30	kV
		human body model (MIL-STD-883)		-	10	kV

[1] Device stressed with non-repetitive current pulses (8/20 µs exponential decay waveform according to IEC 61000-4-5).
[2] Measured from pin 1 or 2 to pin 3.
[3] Measured from pin 1 and 2 to pin 3.
[4] Device stressed with ten non-repetitive ESD pulses.

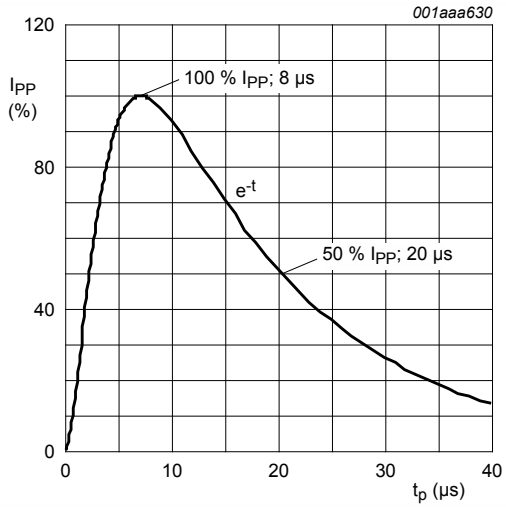


Fig. 2. 8/20 µs pulse waveform according to IEC 61000-4-5

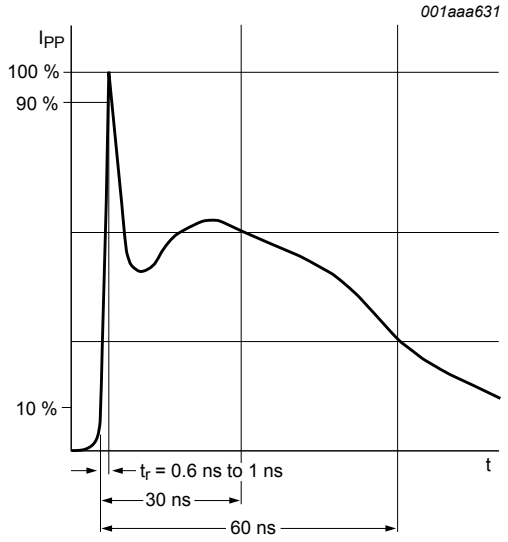


Fig. 3. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	5	V
V_{BR}	breakdown voltage	I_R = 5 mA; T_{amb} = 25 °C		5.5	7	9.5	V
I_{RM}	reverse leakage current	V_R = 5 V; T_{amb} = 25 °C	[1]	-	1	50	nA
C_d	diode capacitance	f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; single line	[1]	-	35	45	pF
		f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C; combined lines	[2]	-	70	90	pF
V_{CL}	clamping voltage	I_{PP} = 1 A; T_{amb} = 25 °C; t_p = 8/20 µs; single line	[3][1]	-	6.5	8.5	V
		I_{PPM} = 14 A; T_{amb} = 25 °C; t_p = 8/20 µs; single line	[3][1]	-	-	11.5	V
		I_{PPM} = 28 A; T_{amb} = 25 °C; t_p = 8/20 µs; combined lines	[4][2]	-	11.5	-	V
		I_{PPM} = 16 A; T_{amb} = 25 °C; t_p = TLP; single line	[4][1]	-	8.5	-	V
		I_{PPM} = 16 A; T_{amb} = 25 °C; t_p = TLP; combined lines	[4][2]	-	7.6	-	V
R_{dyn}	dynamic resistance	I_R = 10 A; T_{amb} = 25 °C; single line	[4][1]	-	0.12	-	Ω
		I_R = 10 A; T_{amb} = 25 °C; combined lines	[4][2]	-	0.07	-	Ω

[1] Measured from pin 1 or 2 to pin 3.
[2] Measured from pin 1 and 2 to pin 3.
[3] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[4] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

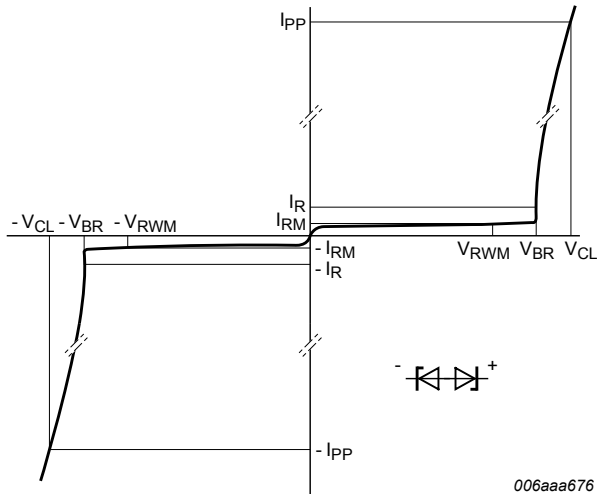
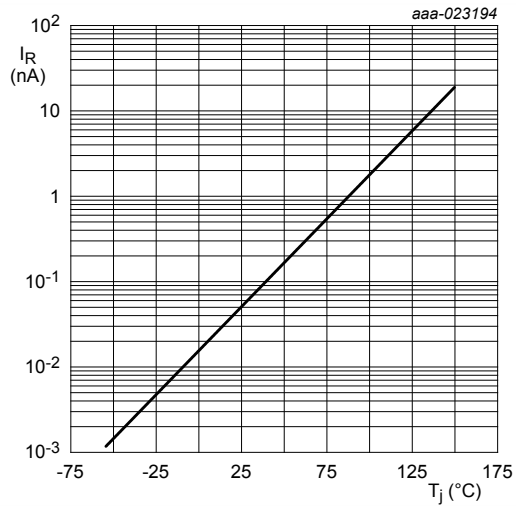
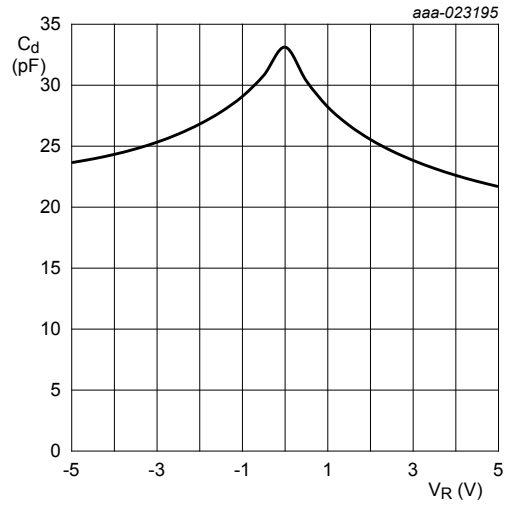


Fig. 4. V-I characteristics for a bidirectional ESD protection diode



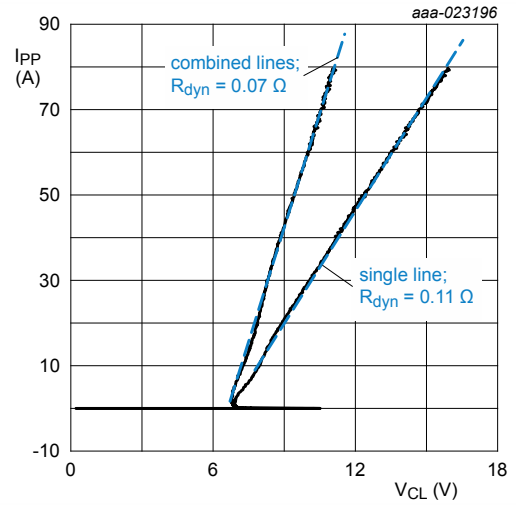
V_{RWM} = 5 V

Fig. 5. Relative variation of reverse leakage current as a function of ambient temperature; typical values



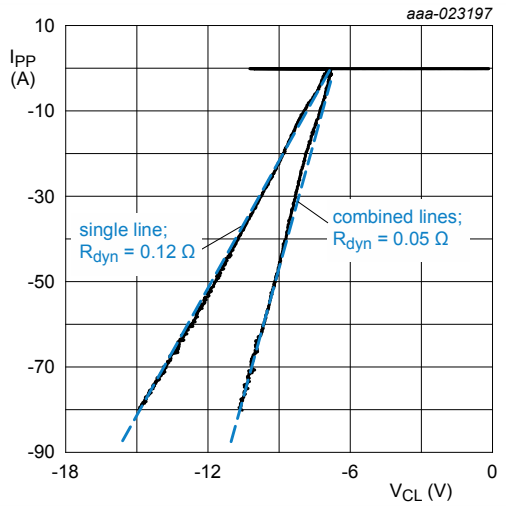
Single line;
f = 1 MHz; V_{GS} = 0 V; T_{amb} = 25 °C

Fig. 6. Diode capacitance as a function of reverse voltage; typical values



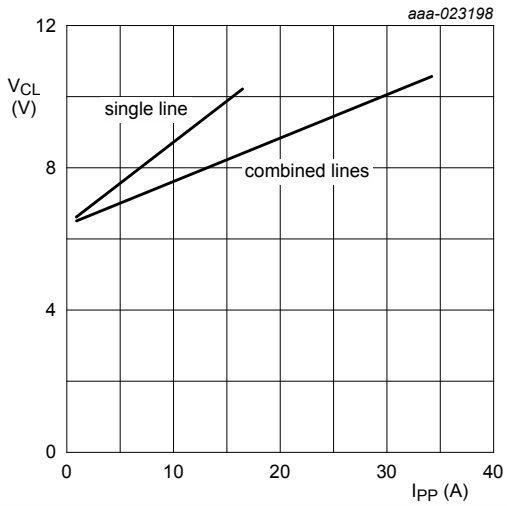
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 7. Dynamic resistance with positive clamping voltage; typical values



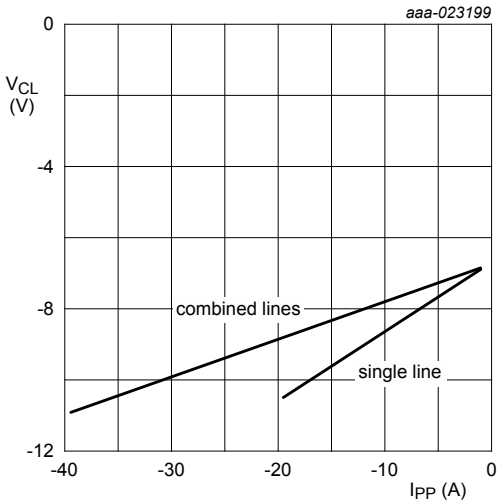
t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 8. Dynamic resistance with negative clamping voltage; typical values



t_p = 8/20 µs; according to IEC 61000-4-5

Fig. 9. Dynamic resistance with positive clamping voltage; typical values



t_p = 8/20 µs; according to IEC 61000-4-5

Fig. 10. Dynamic resistance with negative clamping voltage; typical values

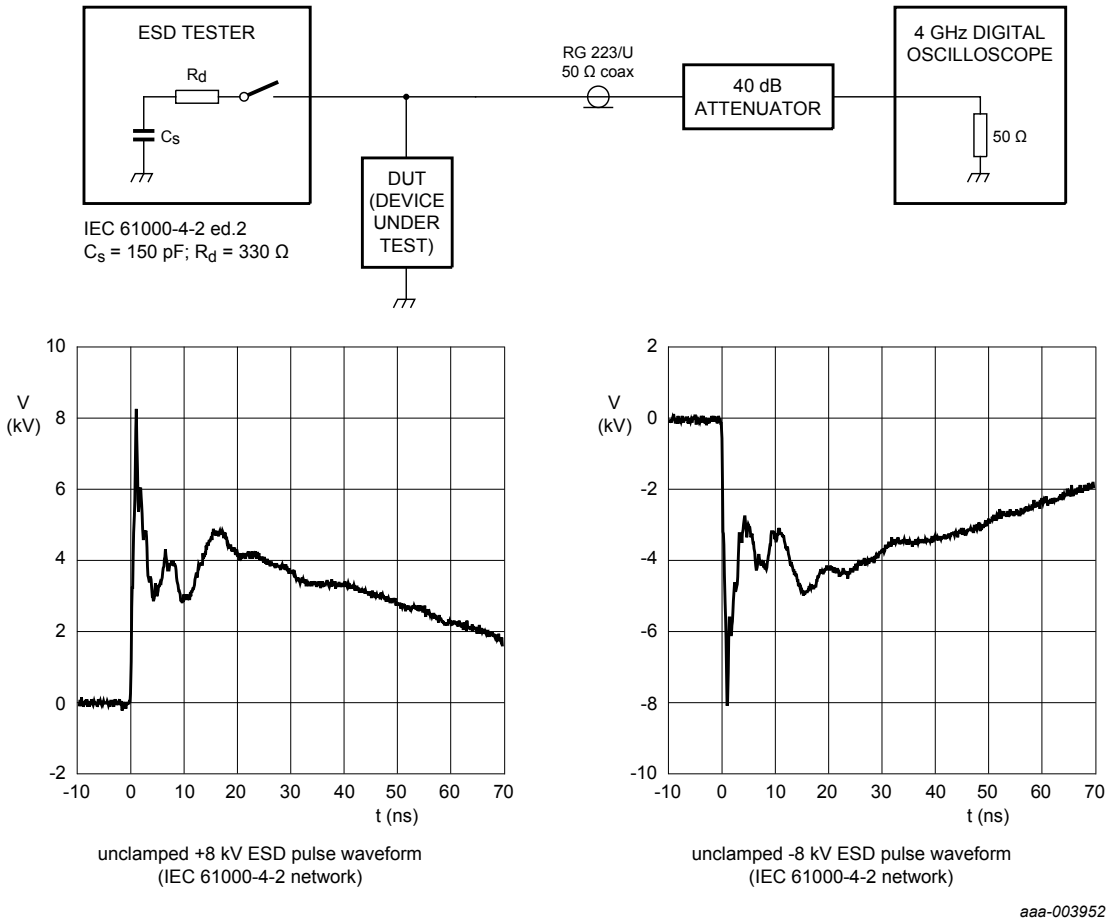


Fig. 11. ESD clamping test setup and waveforms

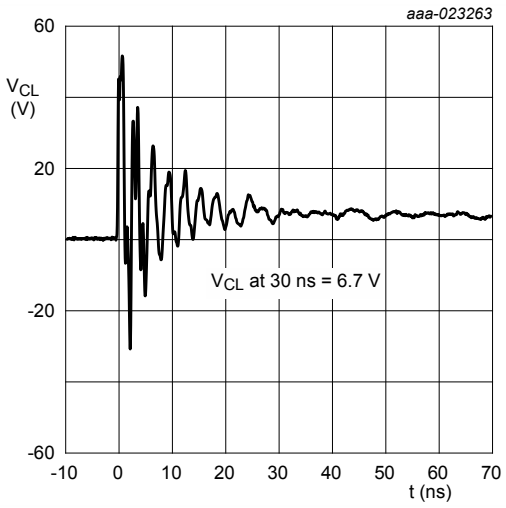


Fig. 12. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

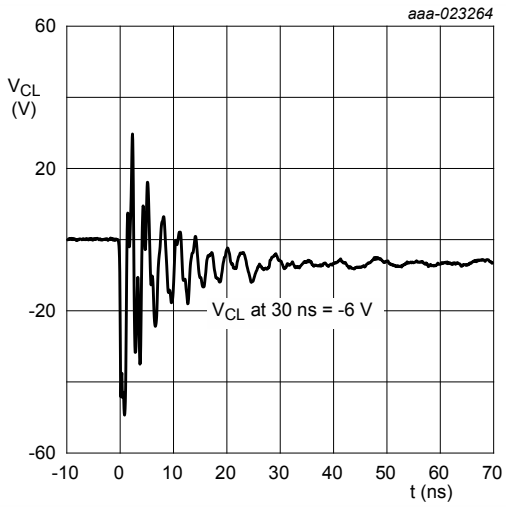


Fig. 13. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

10. Application information

The device is designed for the protection of up to two bidirectional data lines from surge pulses and ESD damage.

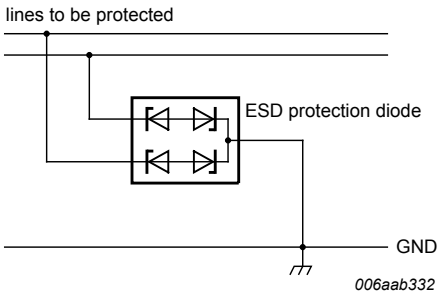


Fig. 14. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

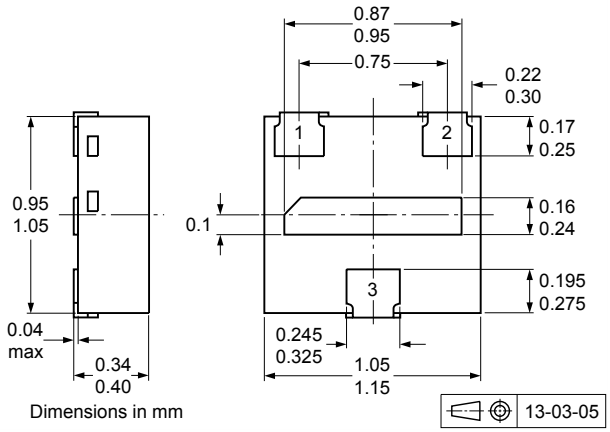


Fig. 15. Package outline DFN1010D-3 (SOT1215)

13. Soldering

Footprint information for reflow soldering of DFN1010D-3 package **SOT1215**

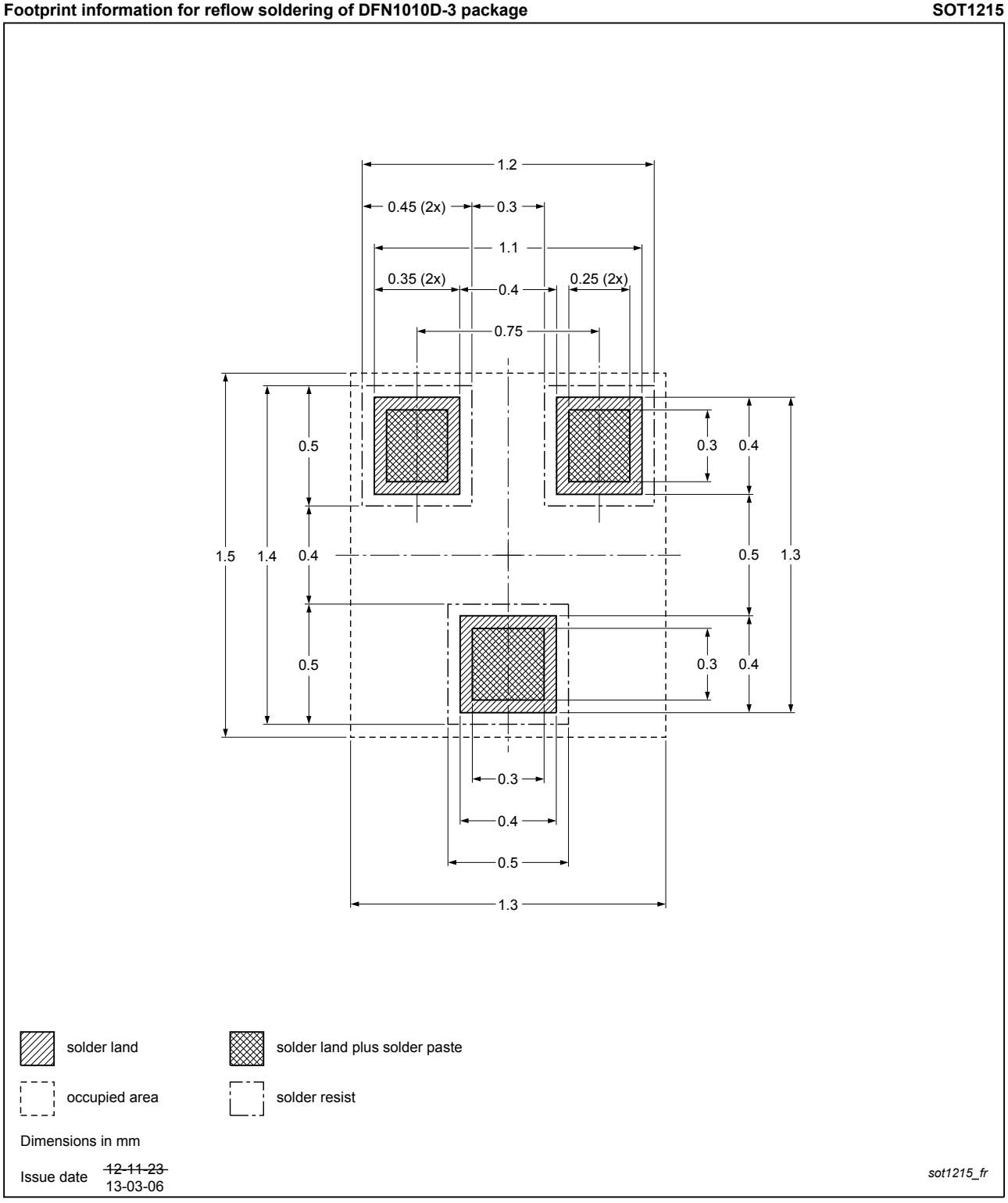


Fig. 16. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0S2BQA v.1	20160601	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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16. Contents

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