

# XP0NG8A

Silicon PNP epitaxial planar type (Tr)  
Silicon epitaxial planar type (SWD)

For digital circuits

■ Features

- Two elements incorporated into one package (Tr + SWD)
- Costs can be reduced through downsizing of the equipment and reduction of the number of parts
- SMini type package allowing easy automatic insertion through tape packing and magazine packing

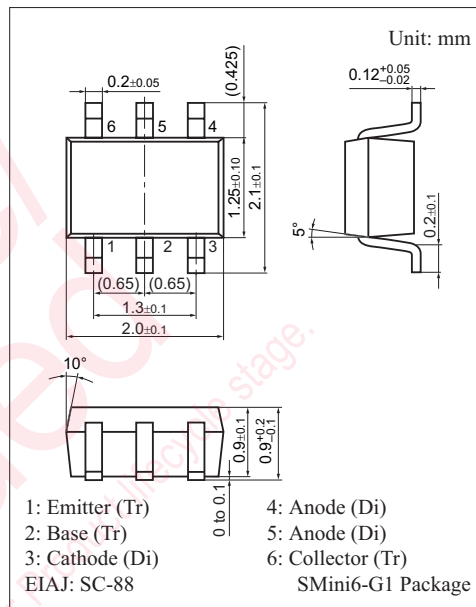
■ Basic Part Number

- UNR211L + MA3X152E

■ Absolute Maximum Ratings  $T_a = 25^\circ\text{C}$

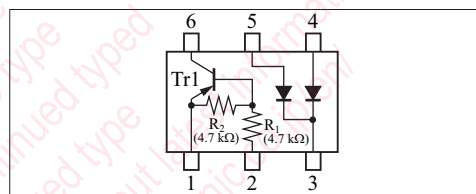
	Parameter	Symbol	Rating	Unit
Tr	Collector-base voltage (Emitter open)	$V_{CBO}$	-50	V
	Collector-emitter voltage (Base open)	$V_{CEO}$	-50	V
	Collector current	$I_C$	-100	mA
SWD	Forward current	$I_F$	100	mA
	Peak forward current	$I_{FM}$	225	mA
	Non-repetitive peak forward surge current *	$I_{FSM}$	500	mA
	Reverse voltage	$V_R$	80	V
	Maximum peak reverse voltage	$V_{RM}$	80	V
Overall	Total power dissipation	$P_T$	150	mW
	Junction temperature	$T_j$	150	$^\circ\text{C}$
	Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Note) \*:  $t = 1\text{ s}$



Marking Symbol: 4D

Internal Connection



■ Electrical Characteristics  $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

• Tr

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	$V_{CBO}$	$I_C = -10 \mu\text{A}, I_E = 0$	-50			V
Collector-emitter voltage (Base open)	$V_{CEO}$	$I_C = -2 \text{ mA}, I_B = 0$	-50			V
Collector-base cutoff current (Emitter open)	$I_{CBO}$	$V_{CB} = -50 \text{ V}, I_E = 0$			-0.1	$\mu\text{A}$
Collector-emitter cutoff current (Base open)	$I_{CEO}$	$V_{CE} = -50 \text{ V}, I_B = 0$			-0.5	$\mu\text{A}$
Emitter-base cutoff current (Collector open)	$I_{EBO}$	$V_{EB} = -6 \text{ V}, I_C = 0$			-2.0	mA
Forward current transfer ratio	$h_{FE}$	$V_{CE} = -10 \text{ V}, I_C = -5 \text{ mA}$	20			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10 \text{ mA}, I_B = -0.3 \text{ mA}$			-0.25	V
Output voltage high-level	$V_{OH}$	$V_{CC} = -5 \text{ V}, V_B = -0.5 \text{ V}, R_L = 1 \text{ k}\Omega$	-4.9			V
Output voltage low-level	$V_{OL}$	$V_{CC} = -5 \text{ V}, V_B = -2.5 \text{ V}, R_L = 1 \text{ k}\Omega$			-0.2	V
Input resistance	$R_1$		-30%	4.7	+30%	$\text{k}\Omega$
Resistance ratio	$R_1 / R_2$		0.8	1.0	1.2	—
Transition frequency	$f_T$	$V_{CB} = -10 \text{ V}, I_E = 1 \text{ mA}, f = 200 \text{ MHz}$		80		MHz

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

• SWD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Forward voltage	$V_F$	$I_F = 100 \text{ mA}$			1.2	V
Reverse voltage	$V_R$	$I_R = 100 \mu\text{A}$	80			V
Reverse current	$I_R$	$V_R = 75 \text{ V}$			0.1	$\mu\text{A}$
Terminal capacitance	$C_t$	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$			2.0	pF
Reverse recovery time	$t_{rr}$	$I_F = 10 \text{ mA}, V_R = 6 \text{ V}, R_L = 100 \Omega,$ $I_{rr} = 0.1 I_R$			3.0	ns

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 measuring methods for diodes.

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