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KA2803B Earth Leakage Detector

Features

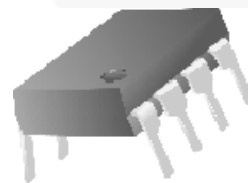
- Low Power Consumption: 5 mW, 100 V/200 V
- Built-In Voltage Regulator
- High-Gain Differential Amplifier
- 0.4 mA Output Current Pulse to Trigger SCRs
- Low External Part Count
- DIP & SOP Packages, High Packing Density
- High Noise Immunity, Large Surge Margin
- Super Temperature Characteristic of Input Sensitivity
- Wide Operating Temperature Range:
T_A = -25°C to +80°C
- Operation from 12 V to 20 V Input

Functions

- Differential Amplifier
- Level Comparator
- Latch Circuit

Description

The KA2803B is designed for use in earth leakage circuit interrupters, for operation directly off the AC line in breakers. The input of the differential amplifier is connected to the secondary coil of ZCT (Zero Current Transformer). The amplified output of differential amplifier is integrated at external capacitor to gain adequate time delay specified in KSC4613. The level comparator generates a high level when earth leakage current is greater than the fixed level.



8-DIP



8-SOP

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
KA2803B	-25 to +80°C	8-Lead, Dual Inline Package (DIP)	Tube

Block Diagram

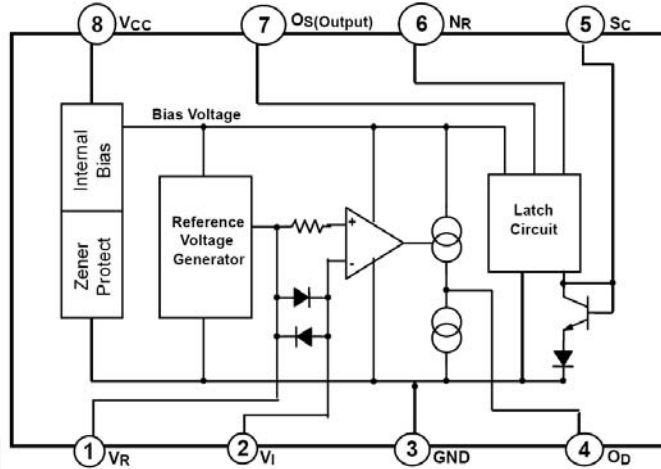


Figure 1. Block Diagram

Application Circuit

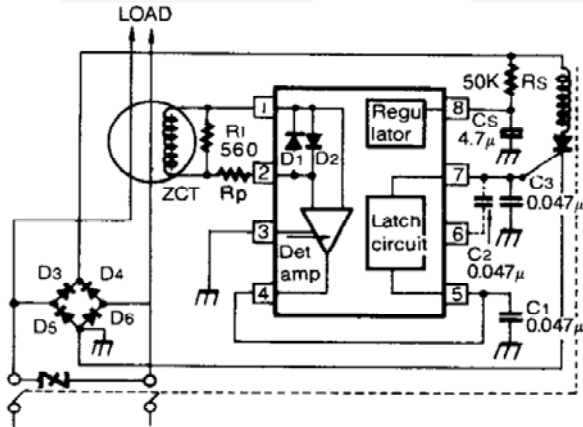


Figure 2. Full-Wave Application Circuit

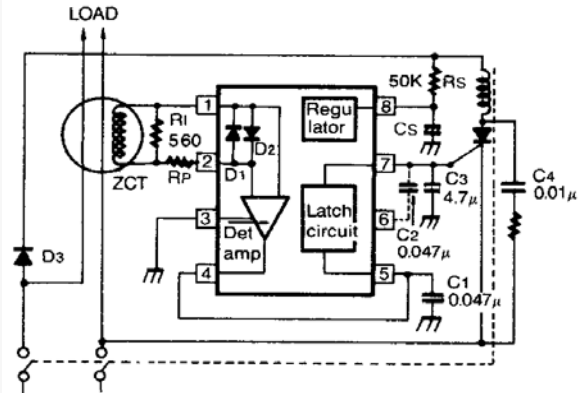


Figure 3. Half-Wave Application Circuit

Application Information

(Refer to full-wave application circuit in Figure 2)

Figure 2 shows the KA2803B connected in a typical leakage current detector system. The power is applied to the V_{CC} terminal (Pin 8) directly from the power line. The resistor R_S and capacitor C_S are chosen so that Pin 8 voltage is at least 12 V. The value of C_S is recommended above 1 μF .

If the leakage current is at the load, it is detected by the zero current transformer (ZCT). The output voltage signal of ZCT is amplified by the differential amplifier of the KA2803B internal circuit and appears as a half-cycle sine wave signal referred to input signal at the output of the amplifier. The amplifier closed-loop gain is fixed about 1000 times with internal feedback resistor to compensate for zero current transformer (ZCT) variations. The resistor R_L should be selected so that the breaker satisfies the required sensing current. The protection resistor R_P is not usually used when high current is injected at the breaker; this resistor should be

used to protect the earth leakage detector IC (KA2803B). The range of R_P is from several hundred Ω to several $\text{k}\Omega$.

Capacitor C_1 is for the noise canceller and a standard value of C_1 is 0.047 μF . Capacitor C_2 is also a noise canceller capacitance, but it is not usually used.

When high noise is present, a 0.047 μF capacitor may be connected between Pins 6 and 7. The amplified signal finally appears at the Pin 7 with pulse signal through the internal latch circuit of the KA2803B. This signal drives the gate of the external SCR, which energizes the trip coil, which opens the circuit breaker. The trip time of the breaker is determined by capacitor C_3 and the mechanism breaker. This capacitor should be selected under 1 μF to satisfy the required trip time. The full-wave bridge supplies power to the KA2803B during both the positive and negative half cycles of the line voltage. This allows the hot and neutral lines to be interchanged.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage		20	V
I_{CC}	Supply Current		8	mA
P_D	Power Dissipation		300	mW
T_L	Lead Temperature, Soldering 10 Seconds		260	°C
T_A	Operation Temperature Range	-25	+80	°C
T_{STG}	Storage Temperature Range	-65	+150	°C

Electrical Characteristics

$T_A = -25^\circ\text{C}$ to $+80^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Test Circuit	Min.	Typ.	Max.	Units	
I_{CC}	Supply Current 1	$V_{CC}=12\text{V}$ $V_R=\text{OPEN}$ $V_I=2\text{V}$	Figure 4			580	μA	
				$T_A = -25^\circ\text{C}$	300	400		530
				$T_A = +25^\circ\text{C}$				480
V_T	Trip Voltage	$V_{CC}=16\text{V}$, $V_R=2\text{V}\sim 2.02\text{V}$, $V_I=2$	Figure 5	14	16	18	mV (ms)	
				Note 1	12.5	14.2		17.0
$I_{O(D)}$	Differential Amplifier Current Current 1	$V_{CC}=16\text{V}$, $V_R\sim V_I=30\text{mV}$, $V_{OD}=1.2\text{V}$	Figure 7	-12	20	-30	μA	
	Differential Amplifier Current Current 2	$V_{CC}=16\text{V}$, $V_{OD}=0.8\text{V}$, V_R , V_I Short= V_P	Figure 8	17	27	37		
I_O	Output Current	$V_{SC}=1.4\text{V}$, $V_{OS}=0.8\text{V}$, $V_{CC}=16.0\text{V}$	Figure 9	$T_A = -25^\circ\text{C}$	200	400	800	μA
				$T_A = +25^\circ\text{C}$	200	400	800	
				$T_A = +80^\circ\text{C}$	100	300	600	
V_{SCON}	Latch-On Voltage	$V_{CC}=16\text{V}$	Figure 10	0.7	1.0	1.4	V	
I_{SCON}	Latch Input Current	$V_{CC}=16\text{V}$	Figure 11	-13	-7	-1	μA	
I_{OSL}	Output Low Current	$V_{CC}=12\text{V}$, $V_{OSL}=0.2\text{V}$	Figure 12	200	800	1400	μA	
V_{IDC}	Differential Input Clamp Voltage	$V_{CC}=16\text{V}$, $I_{IDC}=100\text{mA}$	Figure 13	0.4	1.2	2.0	V	
V_{SM}	Maximum Current Voltage	$I_{SM}=7\text{mA}$	Figure 14	20	24	28	V	
I_{S2}	Supply Current 2	$V_{CC}=12.0\text{V}$, $V_{OSL}=0.6\text{V}$	Figure 15	200	400	900	μA	
V_{SOFF}	Latch-Off Supply Voltage	$V_{OS}=12.0\text{V}$ $V_{SC}=1.8\text{V}$ $I_{IDC}=100.0\text{mA}$	Figure 16	7	8	9	V	
t_{ON}	Response Time	$V_{CC}=16\text{V}$, $V_R\sim V_I=0.3\text{V}$, $1\text{V} < V_X < 5\text{V}$	Figure 17	2	3	4	ms	

Note:

- Guaranteed by design, not tested in production.

Test Circuits

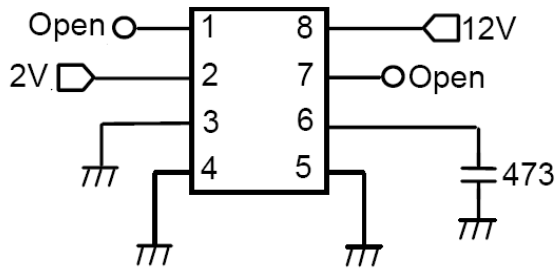


Figure 4. Supply Current 1

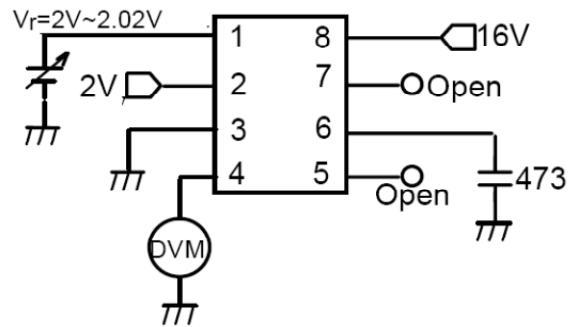
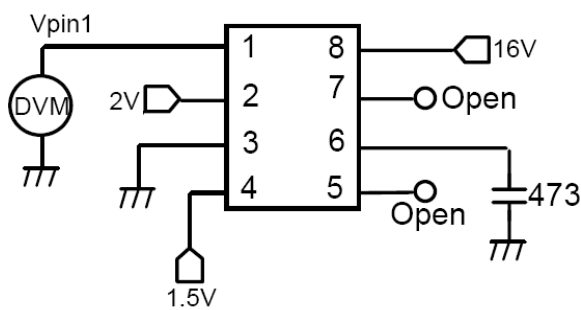


Figure 5. Trip Voltage



$$* V_p = V_{pin1} - 0.03V$$

Figure 6. V_{PN1} for V_P Measurement

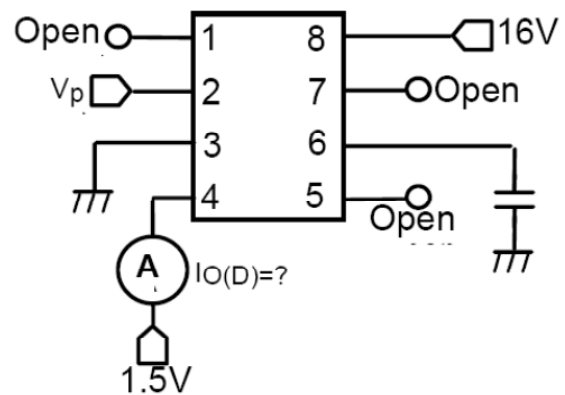


Figure 7. Differential Amplifier Output Current 1

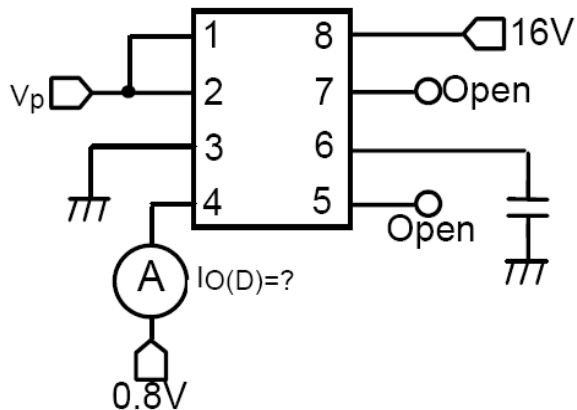


Figure 8. Differential Amplifier Output Current 2

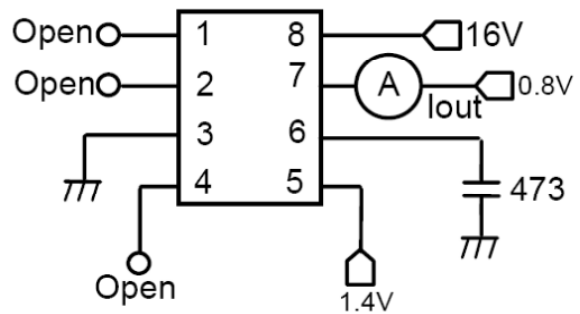


Figure 9. Output Current

Test Circuits (Continued)

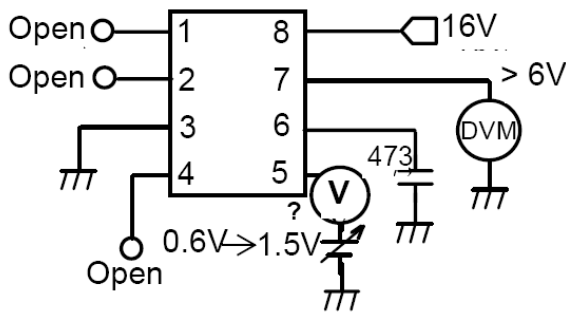


Figure 10. Latch-On Voltage

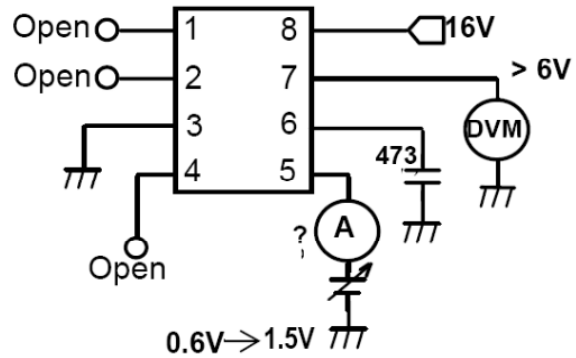


Figure 11. Latch Input Current

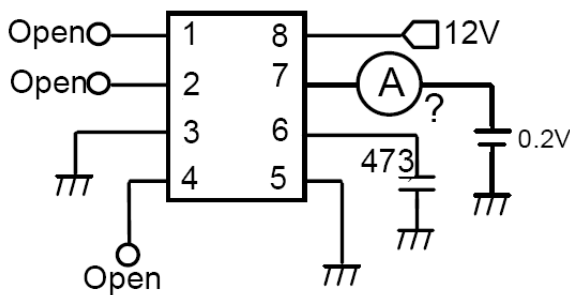


Figure 12. Output Low Current

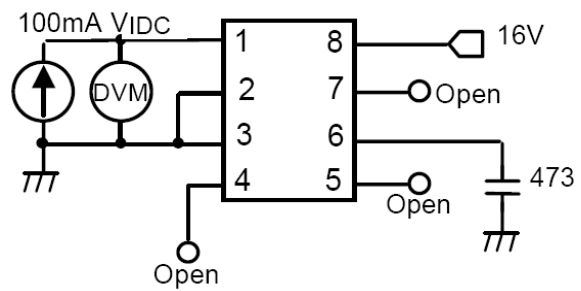


Figure 13. Differential Input Clamp Voltage

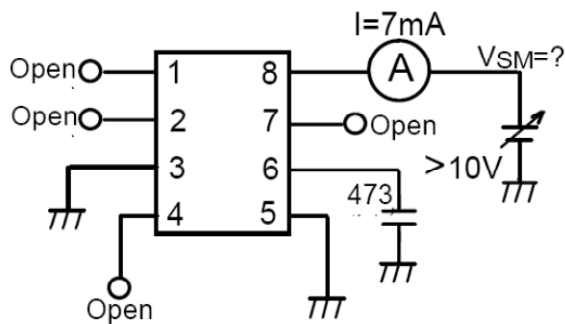


Figure 14. Maximum Current Voltage

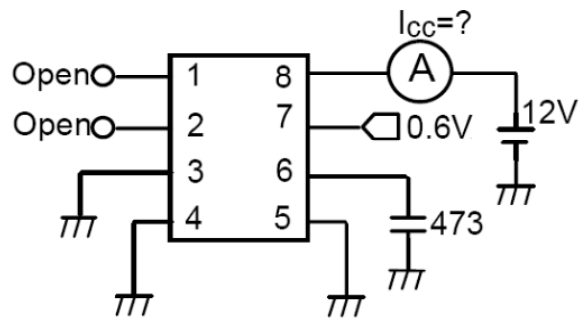


Figure 15. Supply Current 2

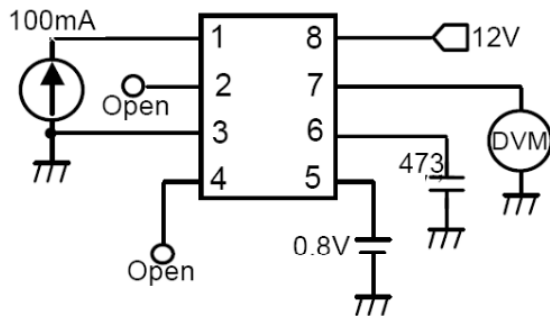


Figure 16. Latch-Off Supply Voltage

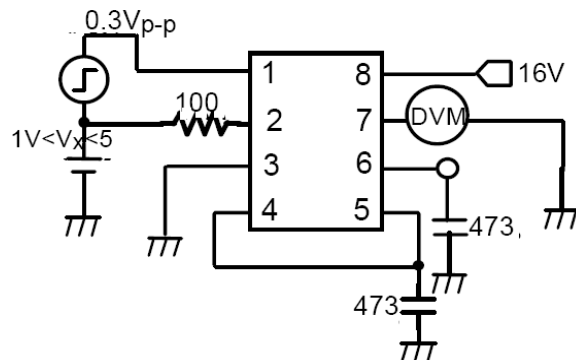


Figure 17. Response Time

Typical Performance Characteristics

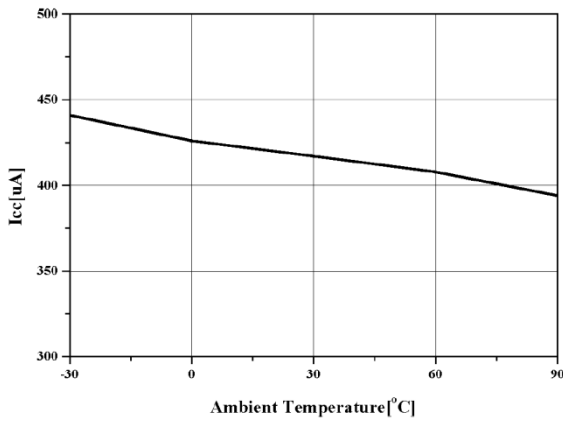


Figure 18. Supply Current

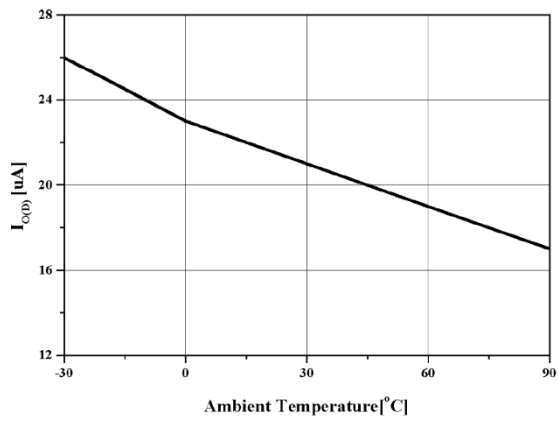


Figure 19. Differential Amplifier Output Current
($V_R - V_I = 30 \text{ mV}$, $V_{OD} = 1.2 \text{ V}$)

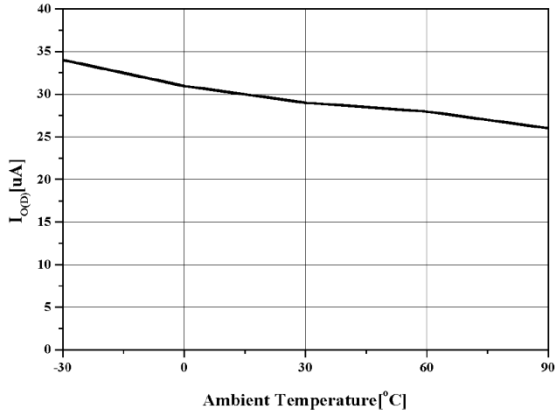


Figure 20. Differential Amplifier Output Current
(V_R , $V_I = V_P$, $V_{OD} = 0.8 \text{ V}$)

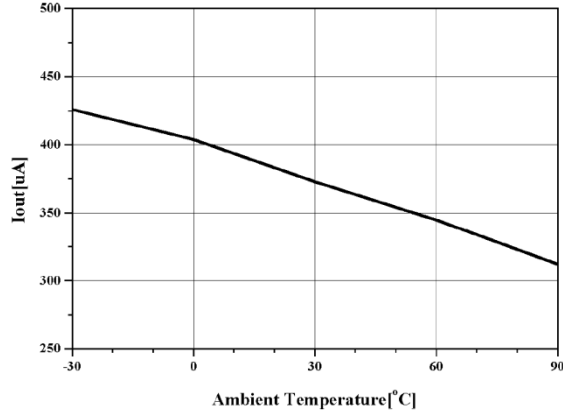


Figure 21. Output Current

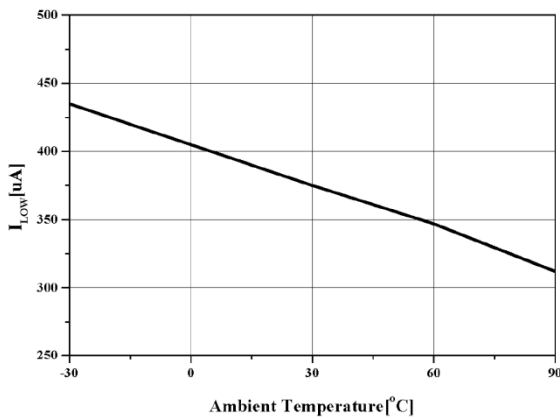


Figure 22. Output Low Current

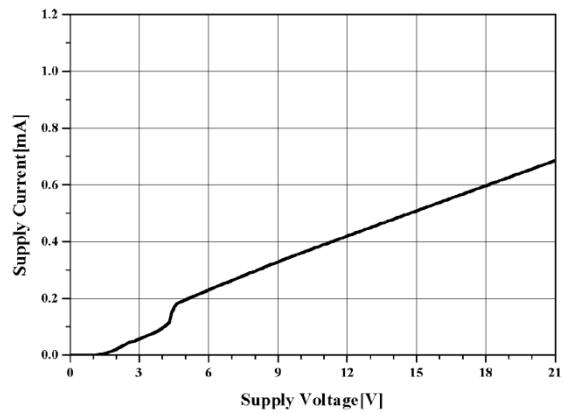


Figure 23. V_{CC} Voltage vs. Supply Current 1

Typical Performance Characteristics (Continued)

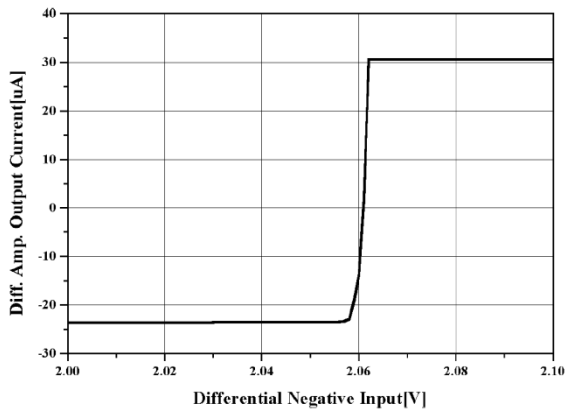


Figure 24. Differential Amplifier Output Current 1

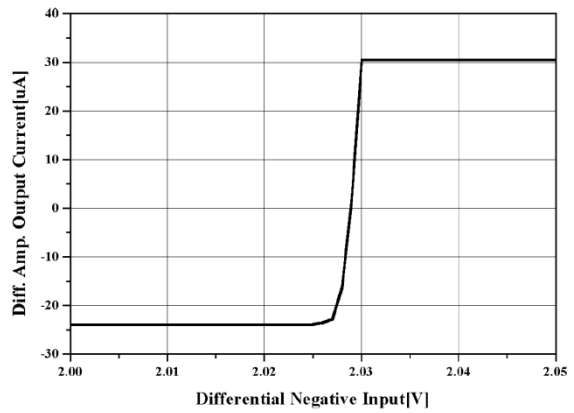


Figure 25. Differential Amplifier Output

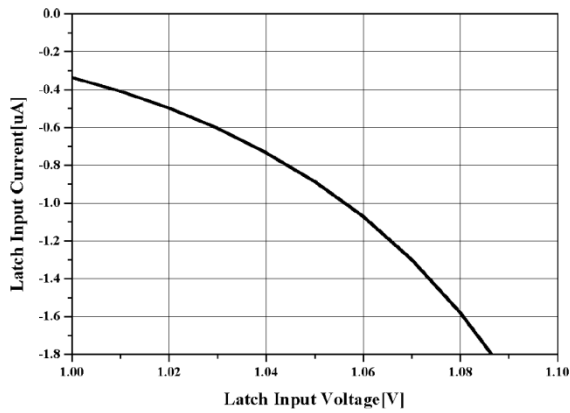


Figure 26. Latch Input Current

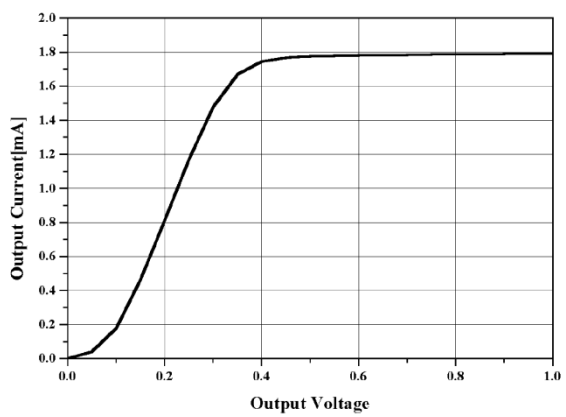


Figure 27. Output Low Current

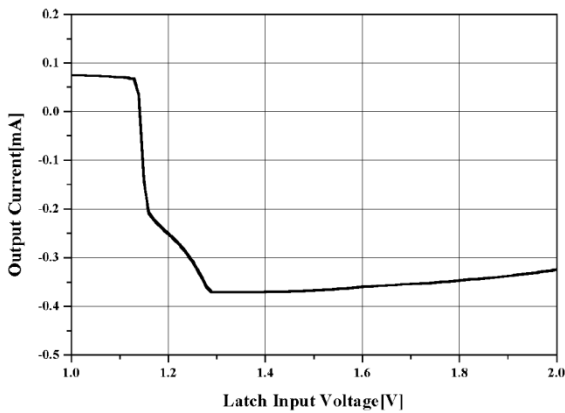


Figure 28. Output Current

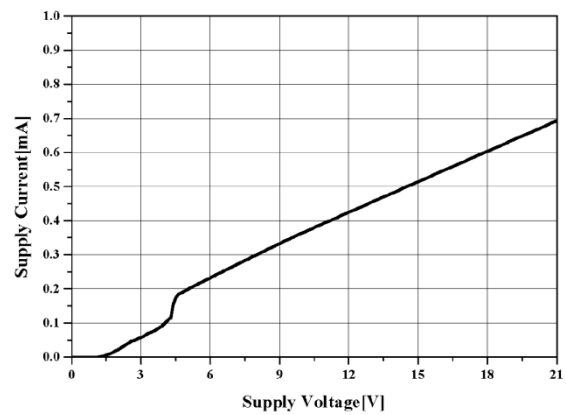


Figure 29. V_{CC} Voltage vs. Supply Current 2

Typical Performance Characteristics (Continued)

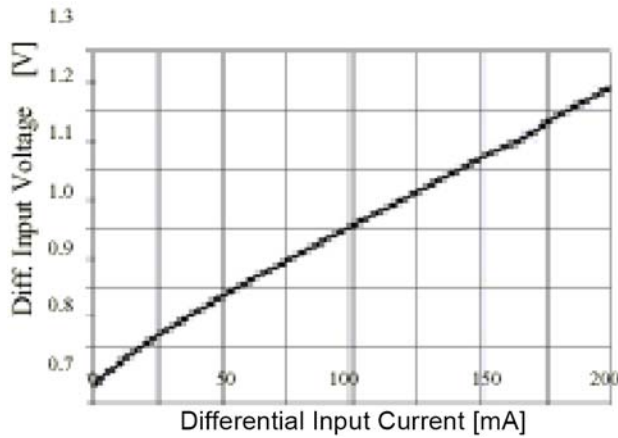


Figure 30. Differential Input Clamp Voltage

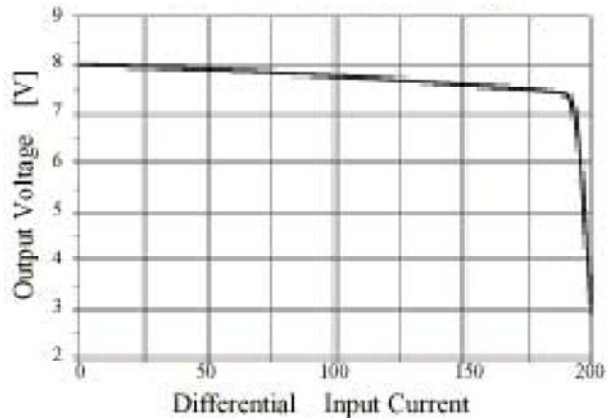


Figure 31. Latch-Off Supply Voltage

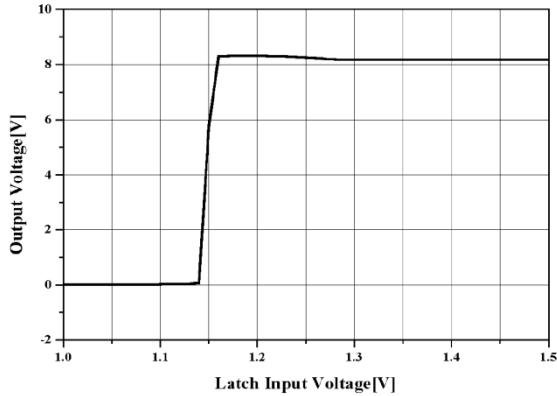


Figure 32. Latch-On Input Voltage

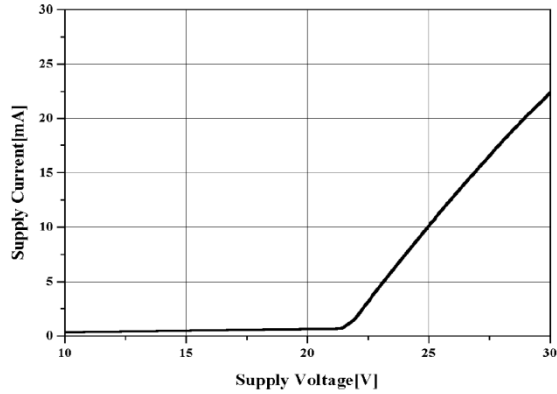


Figure 33. Maximum Supply

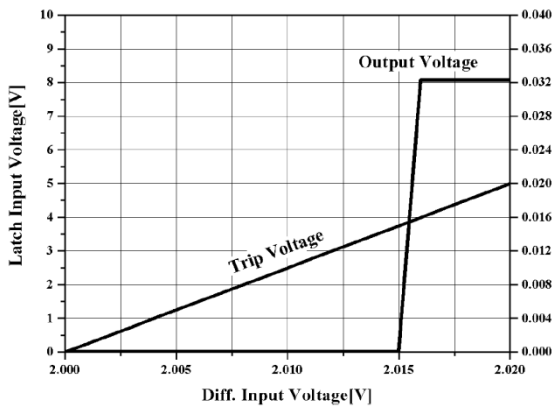


Figure 34. Trip and Output

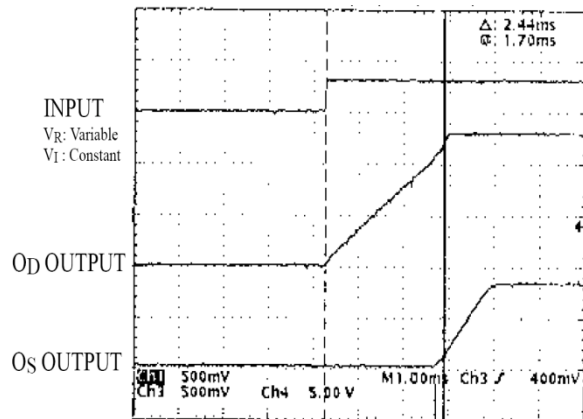
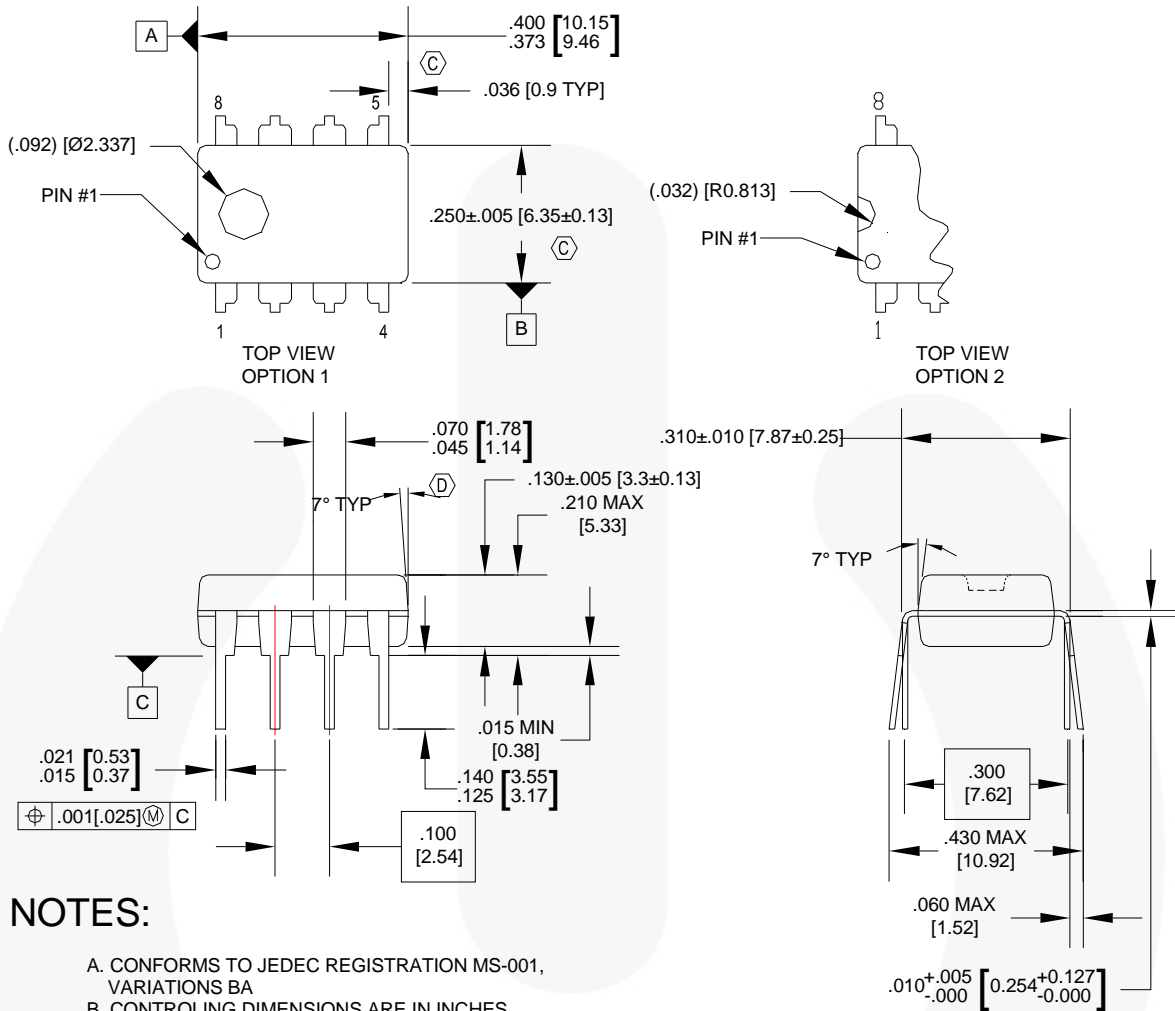


Figure 35. Output Response Time

Physical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS BA
- B. CONTROLLING DIMENSIONS ARE IN INCHES
REFERENCE DIMENSIONS ARE IN MILLIMETERS
- C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
- D. DOES NOT INCLUDE DAMBAR PROTRUSIONS.
DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 INCHES OR 0.25MM.
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

N08EREVG

Figure 36.8-Lead, Dual Inline Package (DIP)

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Physical Dimensions

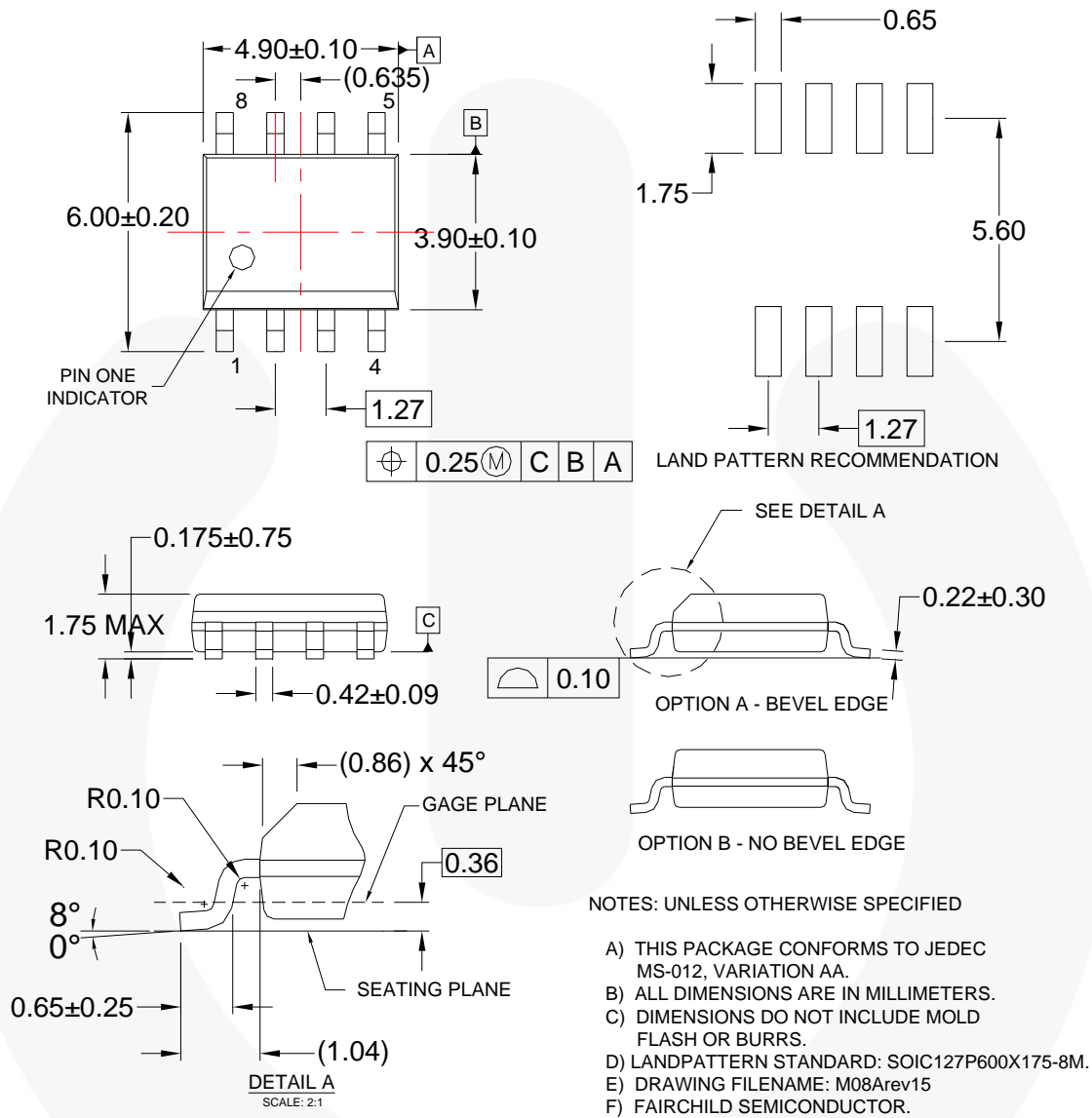


Figure 37.8-Lead, Small Outline Package (SOP)

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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