

# FDMS8848NZ

## N-Channel PowerTrench® MOSFET

40 V, 49 A, 3.1 mΩ

### Features

- Max  $r_{DS(on)}$  = 3.1 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 22.8\text{ A}$
- Max  $r_{DS(on)}$  = 5.1 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 17.5\text{ A}$
- Advanced Package and Silicon combination for low  $r_{DS(on)}$  and high efficiency
- MSL1 robust package design
- RoHS Compliant

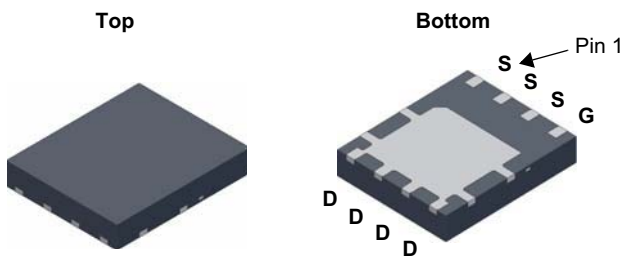


### General Description

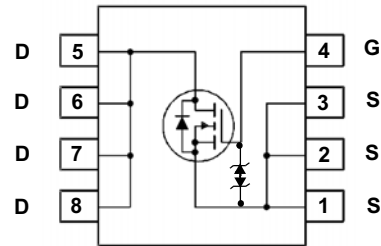
The FDMS8848NZ has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance.

### Applications

- Computing VR & IMVP Vcore
- Secondary Side Synchronous Rectifier
- POL DC/DC Converter
- Oring FET/ Load Switching



Power 56



### MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	49	A
	-Continuous (Silicon limited) $T_C = 25\text{ °C}$	143	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	22.8	
	-Pulsed	90	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	480	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	104	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8848NZ	FDMS8848NZ	Power 56	13"	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		28		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 22.8\ \text{A}$		2.6	3.1	m $\Omega$
		$V_{GS} = 4.5\ \text{V}, I_D = 17.5\ \text{A}$		3.3	5.1	
		$V_{GS} = 10\ \text{V}, I_D = 22.8\ \text{A}, T_J = 125^\circ\text{C}$		3.8	5.3	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\ \text{V}, I_D = 22.8\ \text{A}$		130		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		6071	8075	pF
$C_{oss}$	Output Capacitance			705	940	pF
$C_{rss}$	Reverse Transfer Capacitance			466	700	pF
$R_g$	Gate Resistance			1.4	2.8	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\ \text{V}, I_D = 22.8\ \text{A}, V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		20	36	ns	
$t_r$	Rise Time			19	35	ns	
$t_{d(off)}$	Turn-Off Delay Time			63	101	ns	
$t_f$	Fall Time			13	24	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$		108	152	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$		57	80	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = 20\ \text{V}, I_D = 22.8\ \text{A}$		17		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			19		nC	

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 2.1\ \text{A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\ \text{V}, I_S = 22.8\ \text{A}$ (Note 2)		0.8	1.3	
$t_{rr}$	Reverse Recovery Time	$I_F = 22.8\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		34	55	ns
$Q_{rr}$	Reverse Recovery Charge			28	45	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\ \text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\ \text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



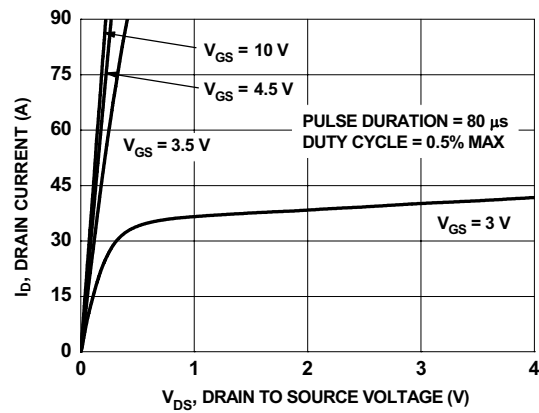
a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\ \text{in}^2$  pad of 2 oz copper.



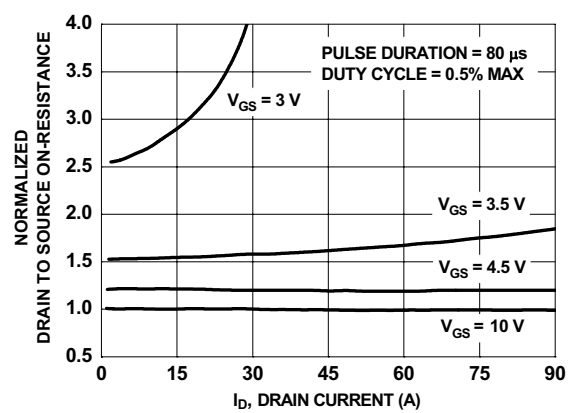
b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width  $< 300\ \mu\text{s}$ , Duty cycle  $< 2.0\%$ .
- Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\ \text{mH}$ ,  $I_{AS} = 31\ \text{A}$ ,  $V_{DD} = 36\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$

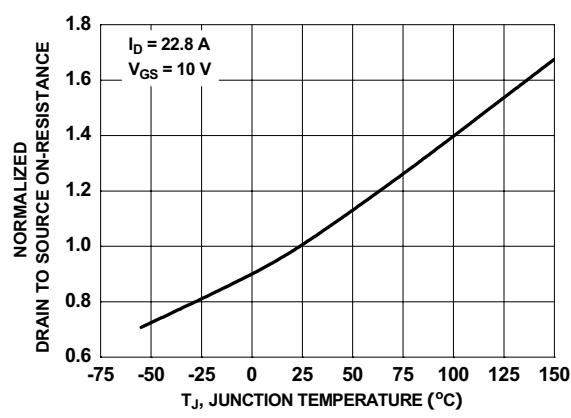
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



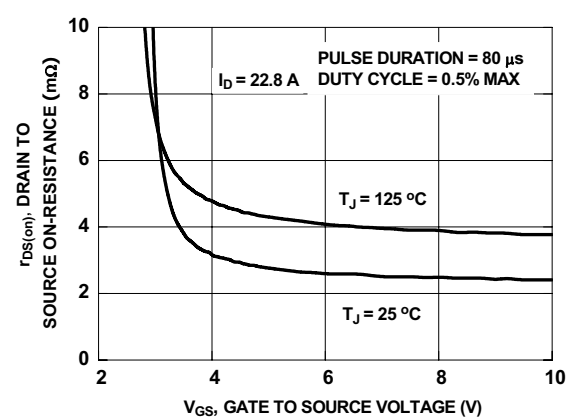
**Figure 1. On Region Characteristics**



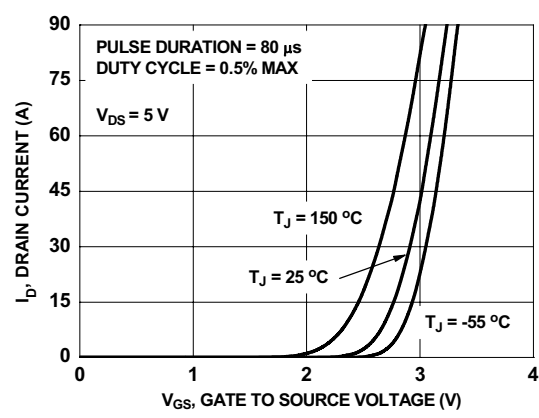
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



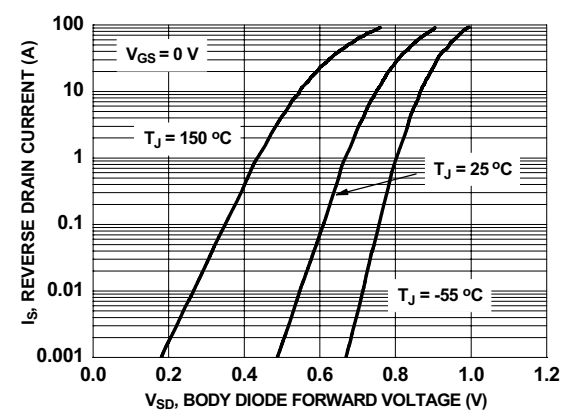
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

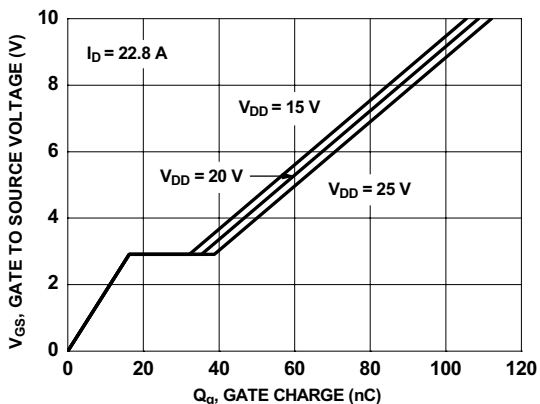


**Figure 5. Transfer Characteristics**

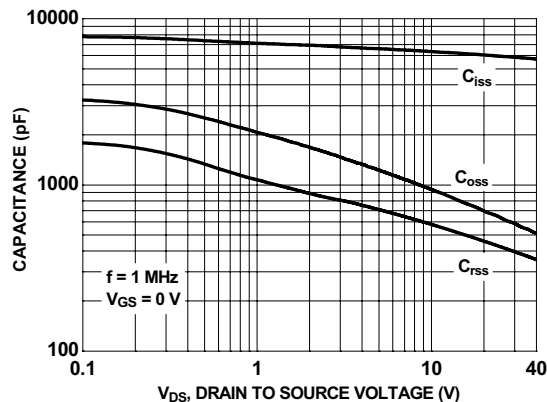


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

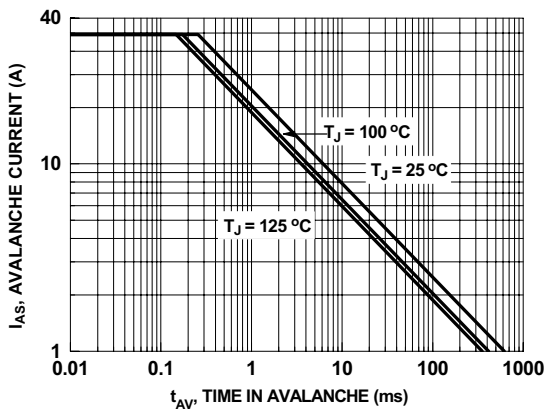
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



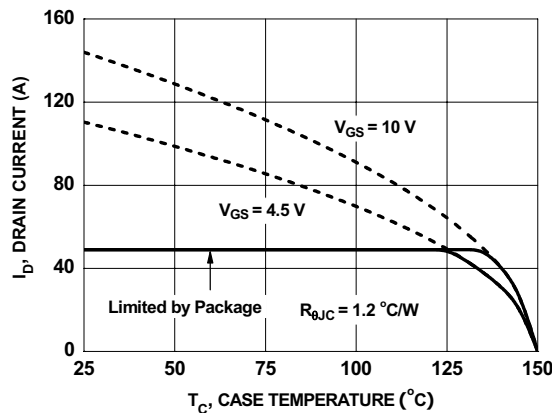
**Figure 7. Gate Charge Characteristics**



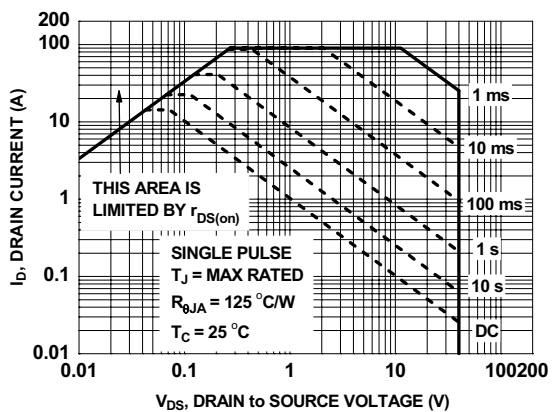
**Figure 8. Capacitance vs Drain to Source Voltage**



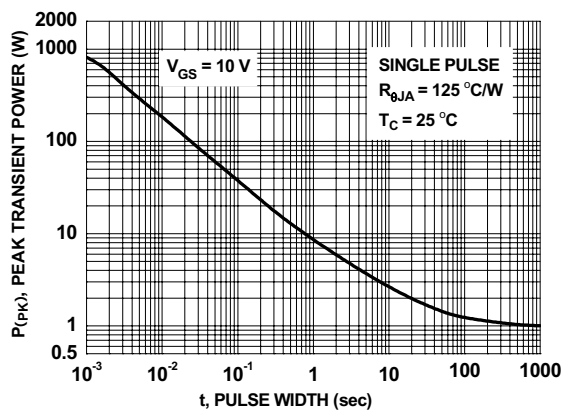
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

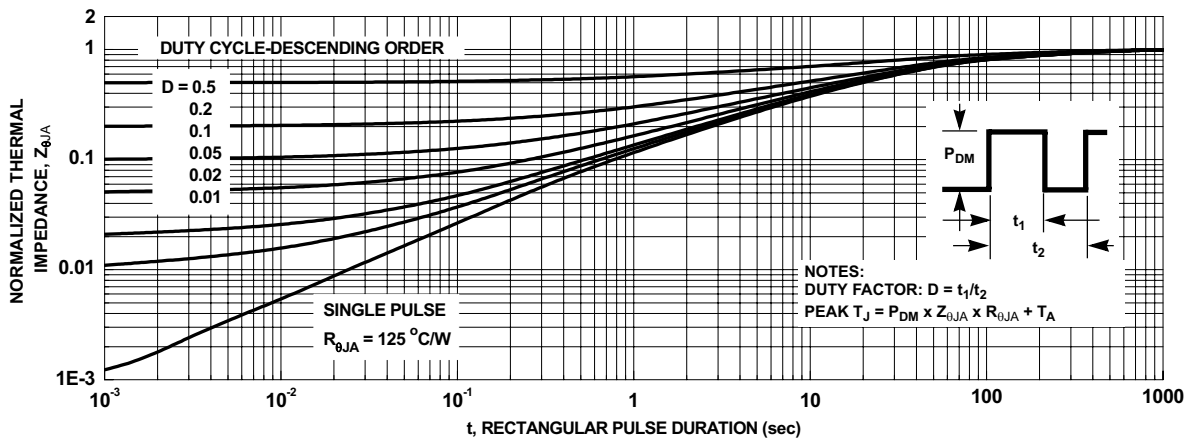


**Figure 11. Forward Bias Safe Operating Area**



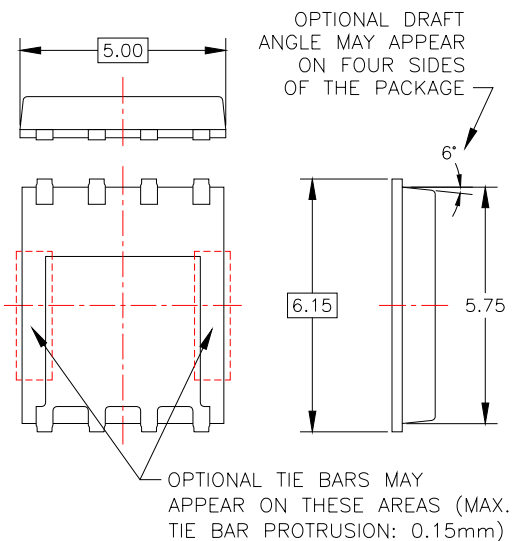
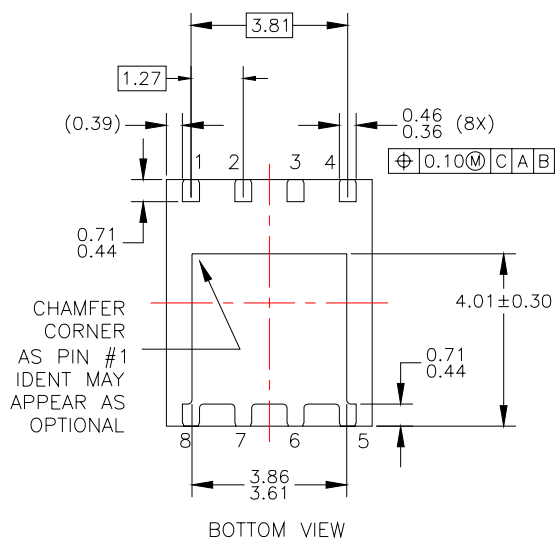
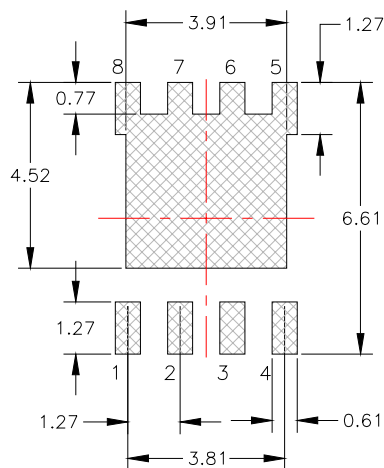
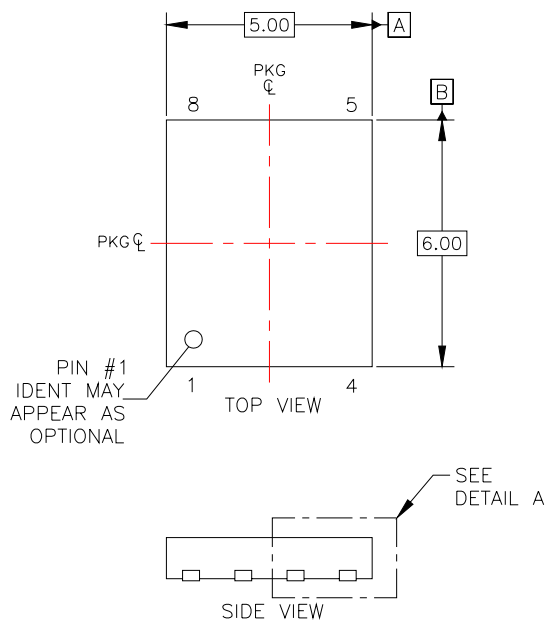
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



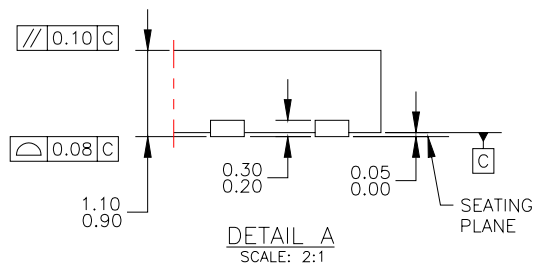
**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED





- A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: POFN08AREV4





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