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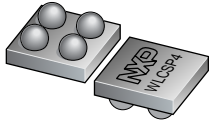
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Kind regards,

Team Nexperia



PMCM4401UPE

20 V, P-channel Trench MOSFET

7 October 2016

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a 4 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Ultra small package: 0.78 × 0.78 × 0.35 mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Battery switch
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

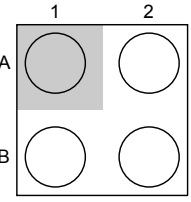
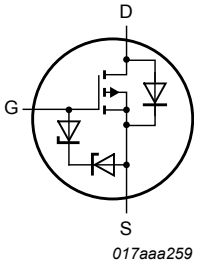
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|---|-----|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j = 25\text{ °C}$ | - | - | -20 | V |
| V_{GS} | gate-source voltage | | -8 | - | 8 | V |
| I_D | drain current | $V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$ | [1] | - | -4 | A |
| Static characteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = -4.5\text{ V}; I_D = -3\text{ A}; T_j = 25\text{ °C}$ | - | 75 | 95 | mΩ |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--|--|
| A1 | G | gate |  <p>Transparent top view WLCSP4 (OL-PMCM4401UPE)</p> |  <p>017aaa259</p> |
| A2 | S | source | | |
| B1 | D | drain | | |
| B2 | S | source | | |

6. Ordering information

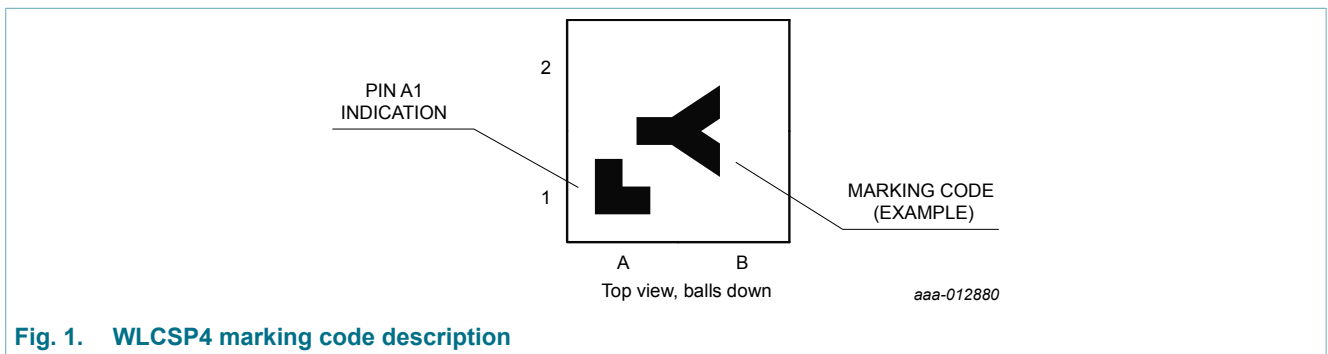
Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|----------------|
| | Name | Description | Version |
| PMCM4401UPE | WLCSP4 | WLCSP4: wafer level chip-size package; 4 bumps (2 x 2) | OL-PMCM4401UPE |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PMCM4401UPE | S |



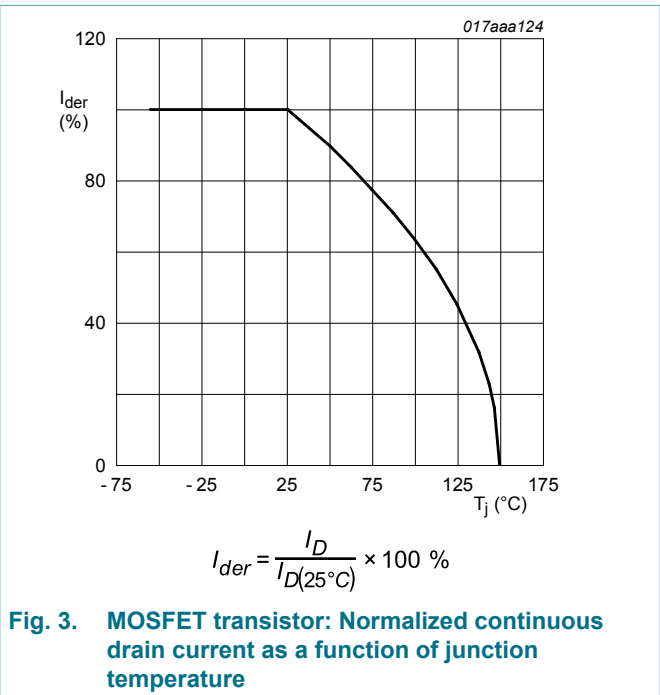
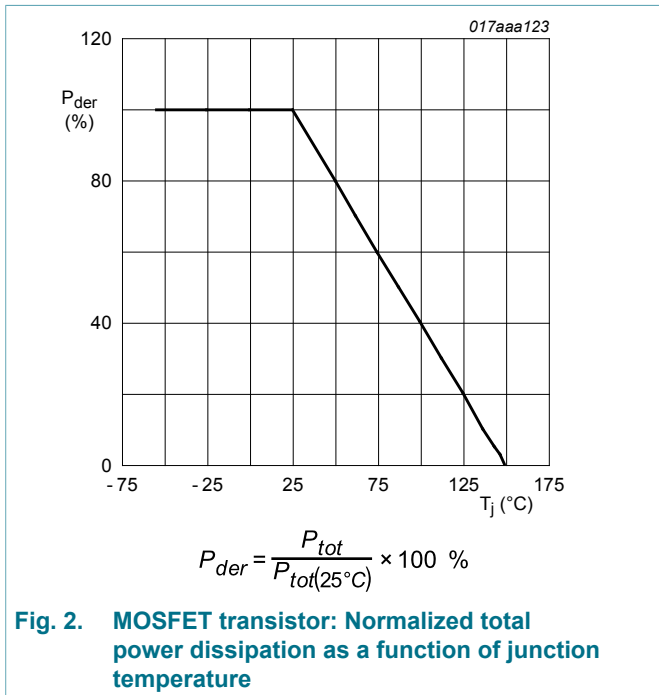
8. Limiting values

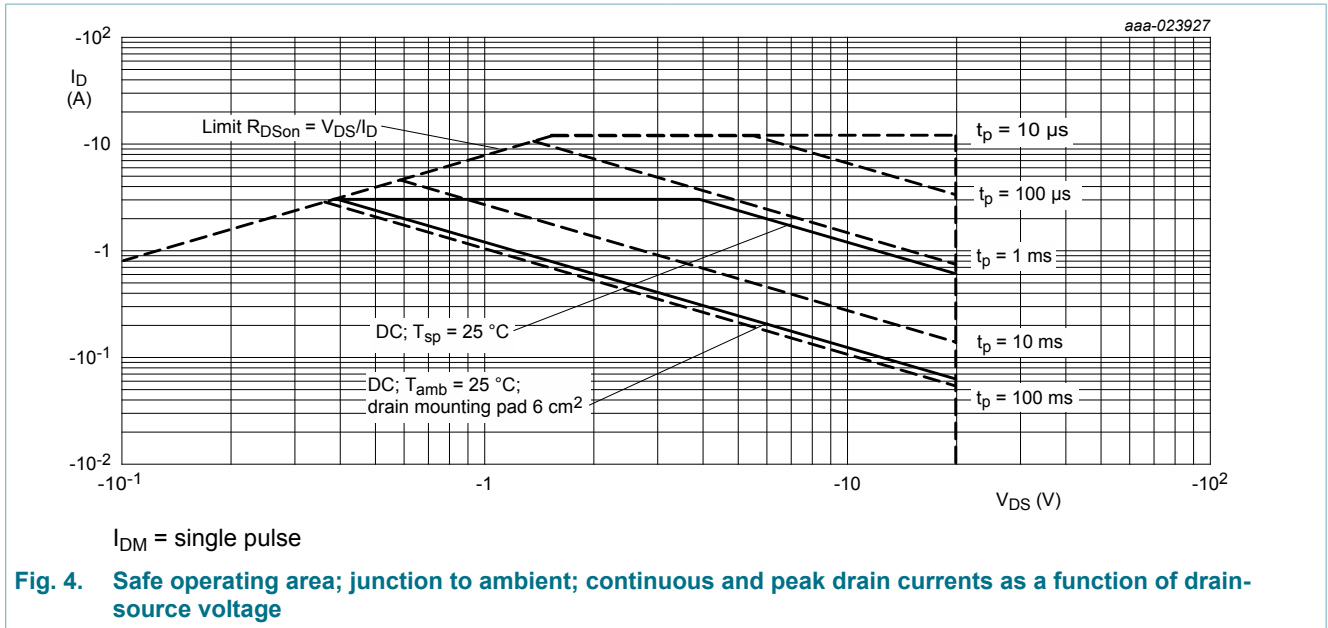
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---------------------------|-------------------------|--|-----|-----|-------|------|
| V _{DS} | drain-source voltage | T _j = 25 °C | | - | -20 | V |
| V _{GS} | gate-source voltage | | | -8 | 8 | V |
| I _D | drain current | V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s | [1] | - | -4 | A |
| | | V _{GS} = -4.5 V; T _{amb} = 25 °C | [1] | - | -3.2 | A |
| | | V _{GS} = -4.5 V; T _{amb} = 100 °C | [1] | - | -2 | A |
| I _{DM} | peak drain current | T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs | | - | -13 | A |
| P _{tot} | total power dissipation | T _{amb} = 25 °C | [2] | - | 400 | mW |
| | | | [1] | - | 1300 | mW |
| | | T _{sp} = 25 °C | | - | 12500 | mW |
| T _j | junction temperature | | | -55 | 150 | °C |
| T _{amb} | ambient temperature | | | -55 | 150 | °C |
| T _{stg} | storage temperature | | | -65 | 150 | °C |
| Source-drain diode | | | | | | |
| I _S | source current | T _{amb} = 25 °C | [1] | - | -1.2 | A |

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|-----------------------|--|----------------------|-----|-----|-----|-----|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | [1] | - | 250 | 300 | K/W |
| | | | [2] | - | 70 | 85 | K/W |
| | | | [3] | - | 85 | 100 | K/W |
| | | in free air; t ≤ 5 s | [3] | - | 50 | 60 | K/W |
| R _{th(j-sp)} | thermal resistance from junction to solder point | | | - | 5 | 10 | K/W |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain, 4-layer, 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

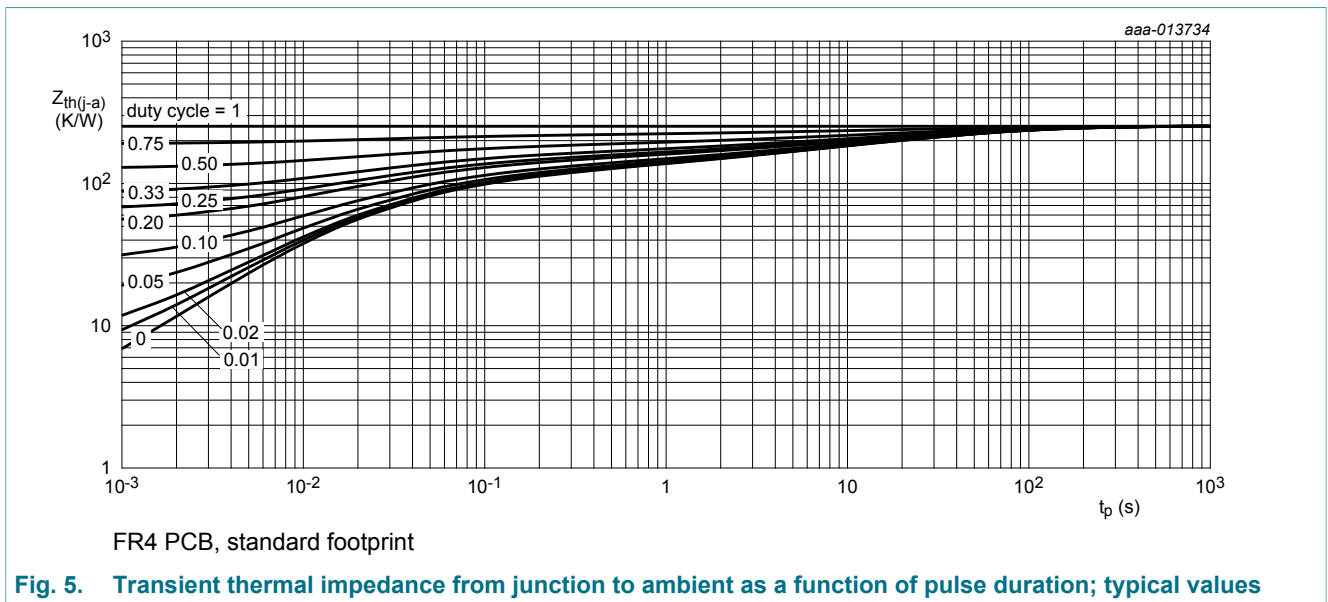
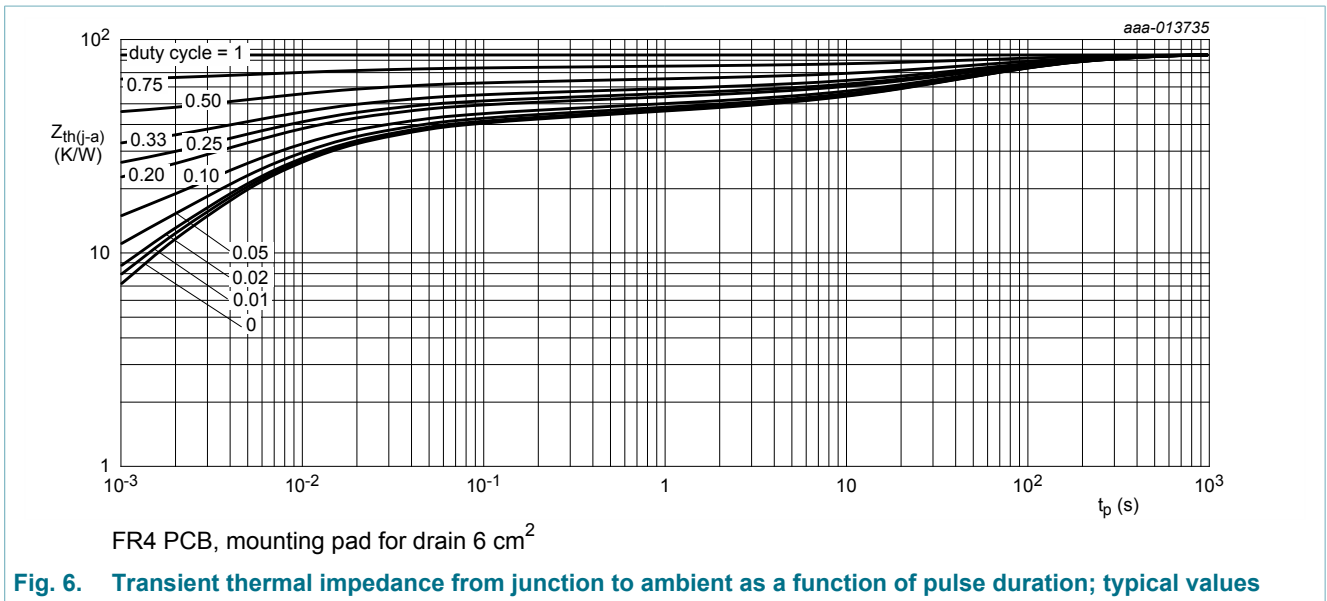


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|--|------|------|------|------------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | -20 | - | - | V |
| V_{GSth} | gate-source threshold voltage | $I_D = -250 \mu A; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$ | -0.4 | -0.6 | -0.9 | V |
| I_{DSS} | drain leakage current | $V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | -1 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | -10 | μA |
| | | $V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | 10 | μA |
| | | $V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | -1 | μA |
| | | $V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | 1 | μA |
| | | $V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | -200 | nA |
| | | $V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | - | 200 | nA |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = -4.5 V; I_D = -3 A; T_j = 25 \text{ }^\circ C$ | - | 75 | 95 | m Ω |
| | | $V_{GS} = -4.5 V; I_D = -3 A; T_j = 150 \text{ }^\circ C$ | - | 100 | 120 | m Ω |
| | | $V_{GS} = -2.5 V; I_D = -2 A; T_j = 25 \text{ }^\circ C$ | - | 95 | 130 | m Ω |
| | | $V_{GS} = -1.8 V; I_D = -0.1 A; T_j = 25 \text{ }^\circ C$ | - | 130 | 190 | m Ω |
| g_{fs} | forward transconductance | $V_{DS} = -6 V; I_D = -3 A; T_j = 25 \text{ }^\circ C$ | - | 10.8 | - | S |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 7 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $V_{DS} = -10 V; I_D = -3 A; V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$ | - | 5.9 | 10 | nC |
| Q_{GS} | gate-source charge | | - | 0.6 | - | nC |
| Q_{GD} | gate-drain charge | | - | 1.7 | - | nC |
| C_{iss} | input capacitance | $V_{DS} = -10 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 420 | - | pF |
| C_{oss} | output capacitance | | - | 64 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 58 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = -10 V; I_D = -3.3 A; V_{GS} = -4.5 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$ | - | 4 | - | ns |
| t_r | rise time | | - | 18 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 31 | - | ns |
| t_f | fall time | | - | 13 | - | ns |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = -1.2 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | -0.8 | -1.2 | V |

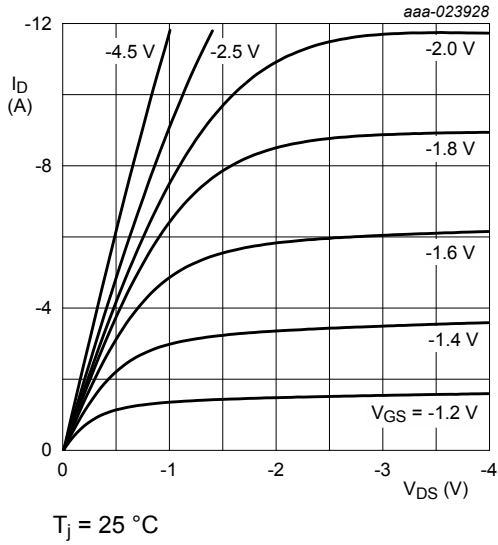


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

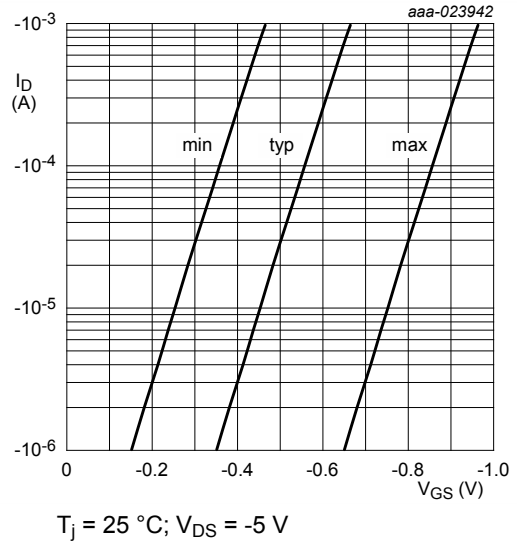


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

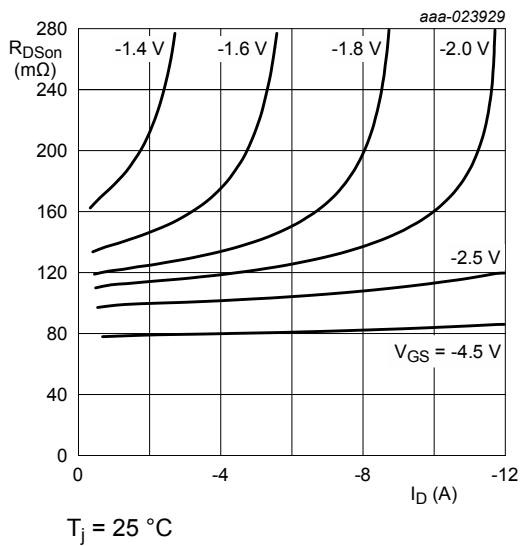


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

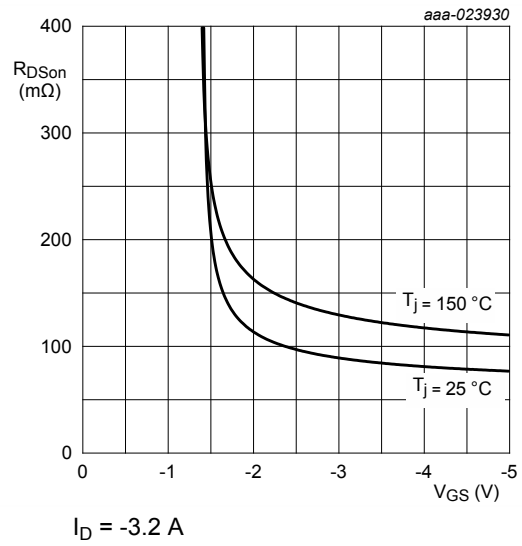


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

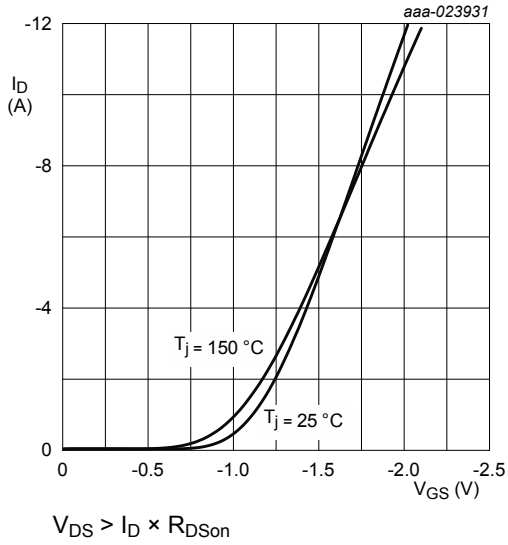


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

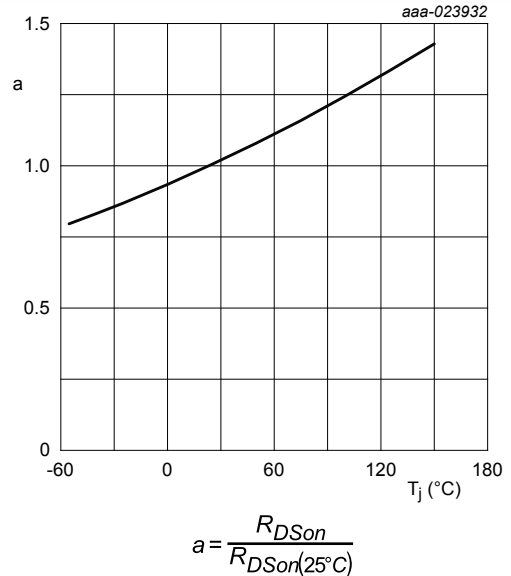


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

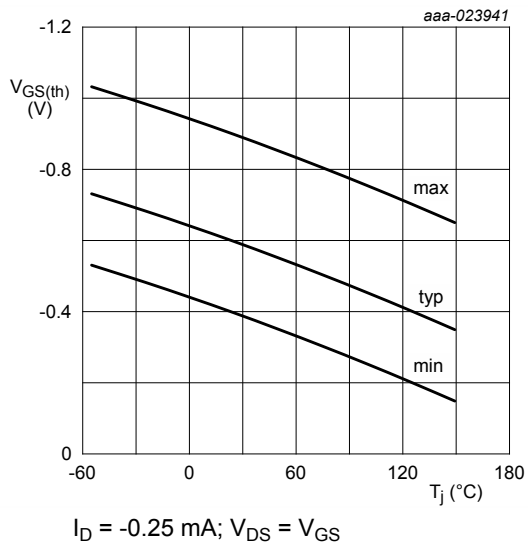


Fig. 13. Gate-source threshold voltage as a function of junction temperature

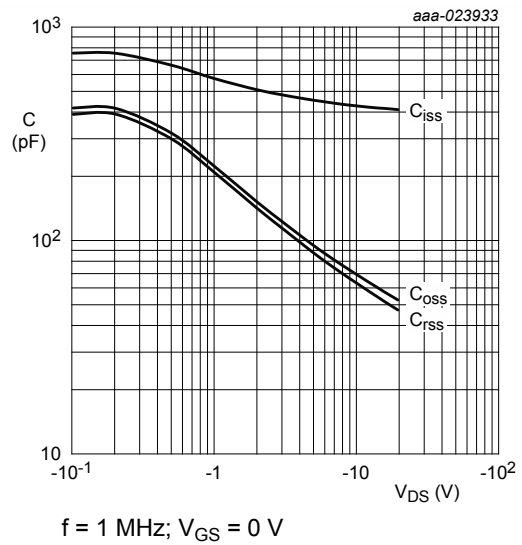
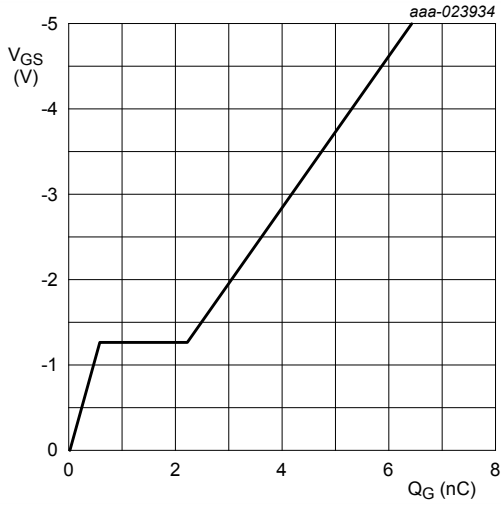


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -3$ A; $V_{DS} = -10$ V; $T_{amb} = 25$ °C

Fig. 15. Gate-source voltage as a function of gate charge; typical values

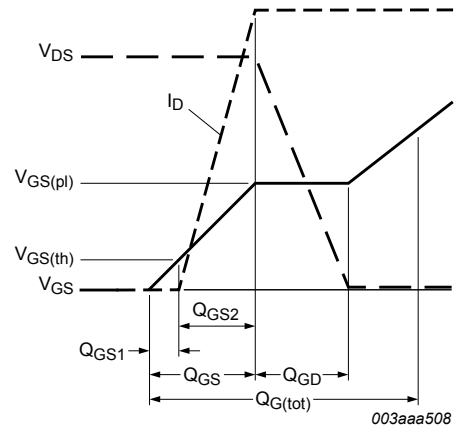
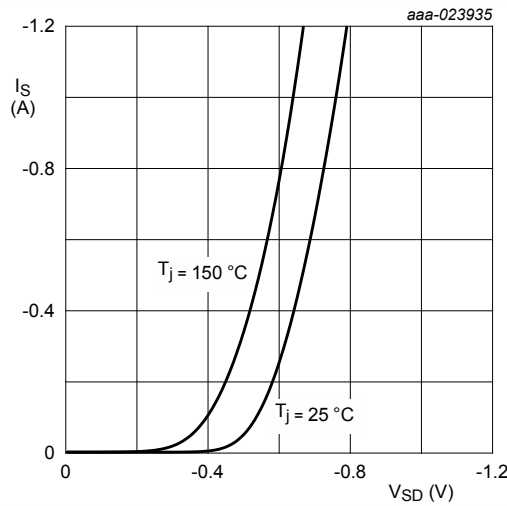


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

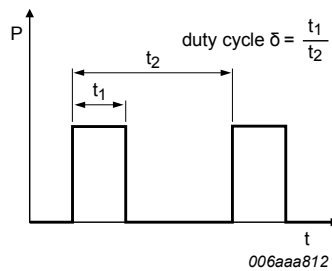


Fig. 18. Duty cycle definition

12. Package outline

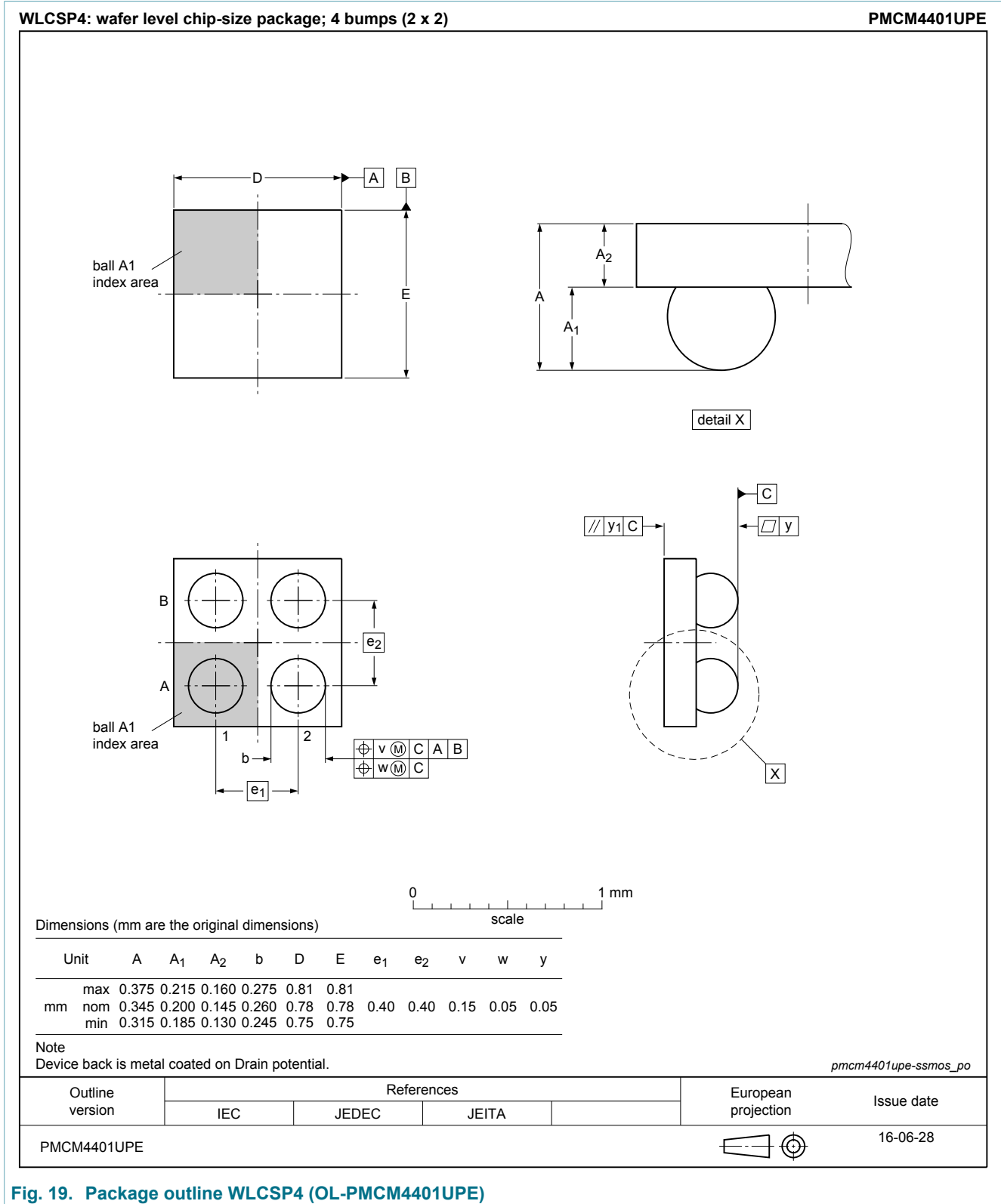
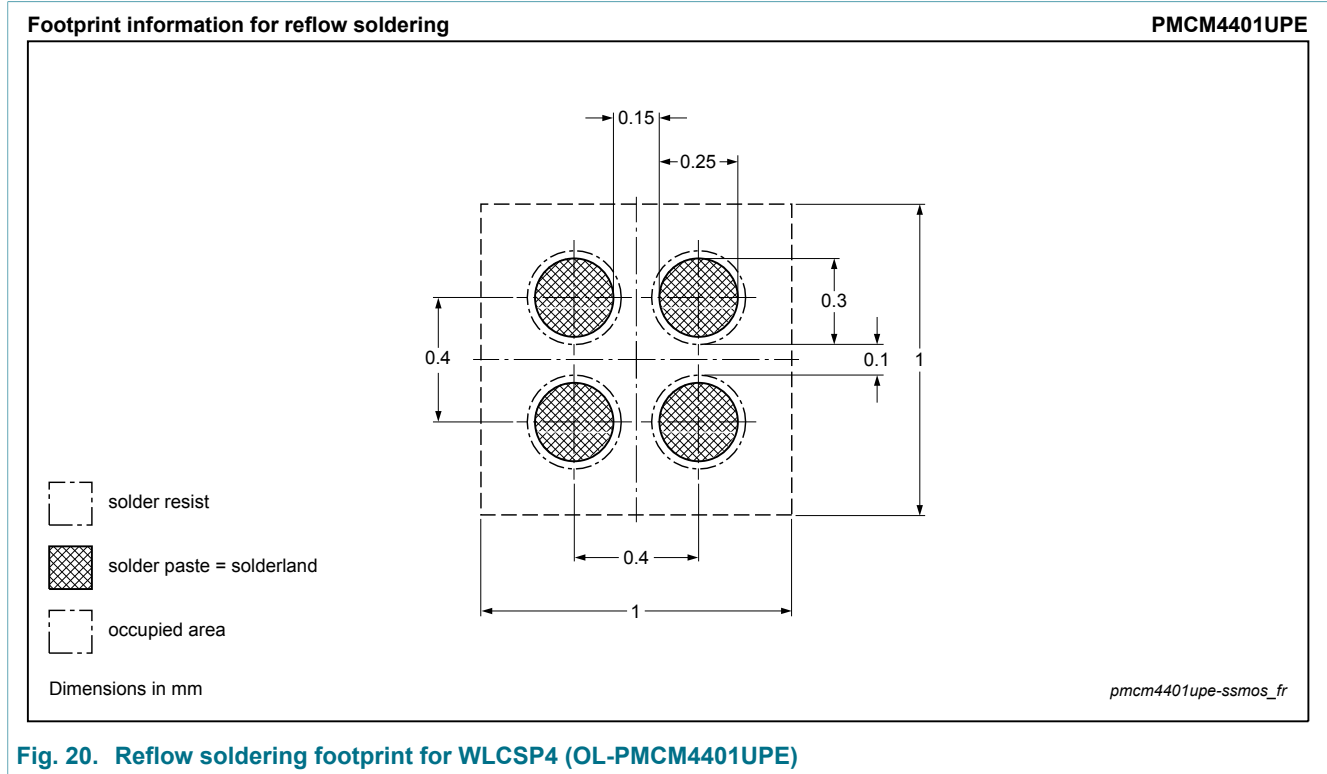


Fig. 19. Package outline WLCSP4 (OL-PMCM4401UPE)

13. Soldering



14. Revision history

Table 8. Revision history

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--|--------------------|---------------|-----------------|
| PMCM4401UPE v.2 | 20161007 | Product data sheet | - | PMCM4401UPE v.1 |
| Modification: | <ul style="list-style-type: none">R_{dson} at $V_{GS} = -4.5$ V; $I_D = -3$ A; $T_j = 25$ °C corrected to 95 mΩ. | | | |
| PMCM4401UPE v.1 | 20160704 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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