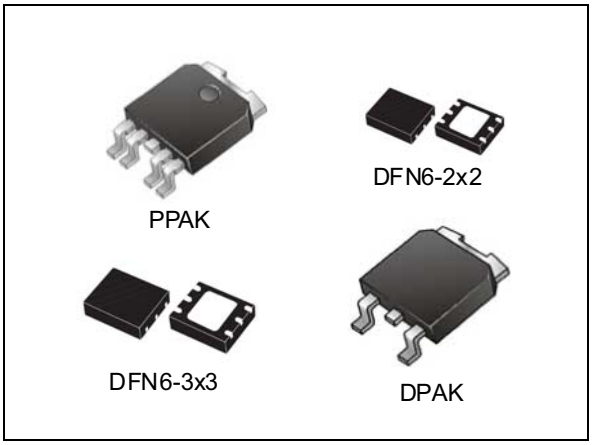
LDF

1 A very low drop voltage regulator

Datasheet - production data



Features

- Input voltage from 2.6 to 16 V
- Very low-dropout voltage (500 mV max. at 1 A load)
- Low quiescent current (200 µA typ. @ 1 A load)
- Available in 1% precision in PPAK and DFN6 packages, 2% in DPAK
- 1 A guaranteed output current
- Wide range of output voltages available on request: adjustable from 0.8 V, fixed up to 12 V in 100 mV steps
- Logic-controlled electronic shutdown
- Power Good (PPAK and DFN packages)
- Fast dynamic response to line and load changes
- Internal current and thermal protections
- Temperature range: -40 °C to 125 °C

Applications

- Computer and laptop
- Battery-powered equipments
- Industrial and medical equipment
- Consumer and set-top box

Description

The LDF is a fast, very low drop linear regulator which operates from an input supply voltage in the range of 2.6 V to 16 V.

It is available in fixed and adjustable output voltage versions, from 0.8 V to 12 V.

The LDF features are: high output precision, very low-dropout voltage, low noise, and low quiescent current, therefore suitable for low voltage microprocessors and memory applications.

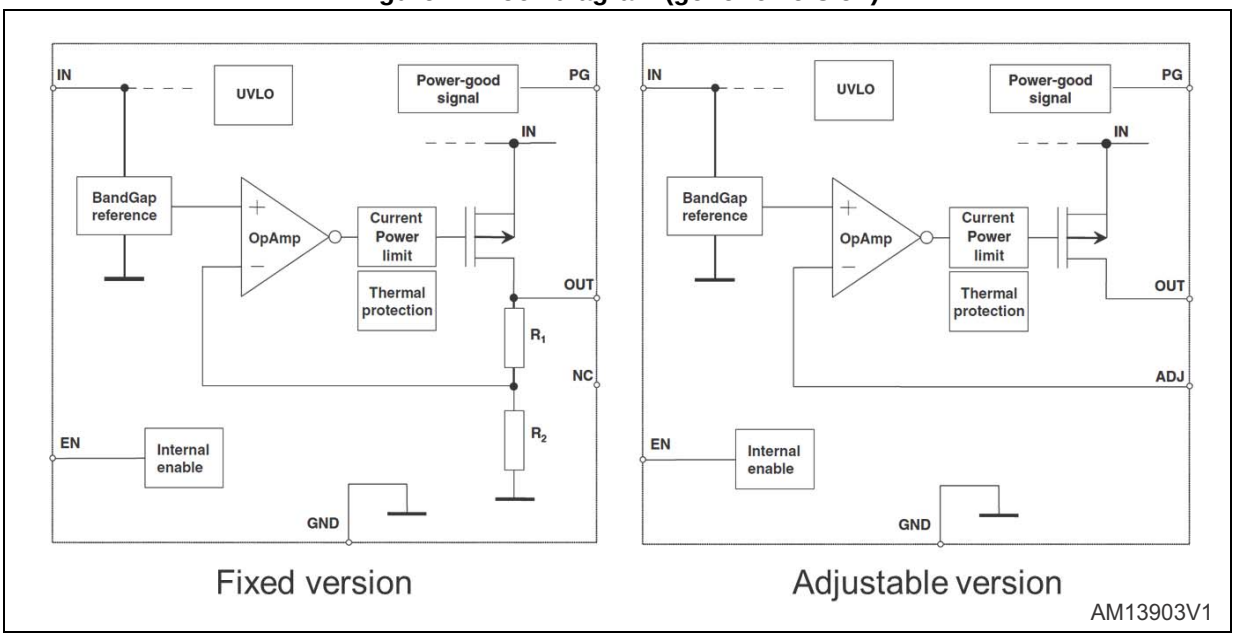
Enable logic control pin and power-good output are featured on PPAK/DFN packages.

Current and thermal protection are provided.

Contents

1 Block diagram

Figure 1. Block diagram (generic version)



2 Pin configuration

Figure 2. Pin connection (top view)

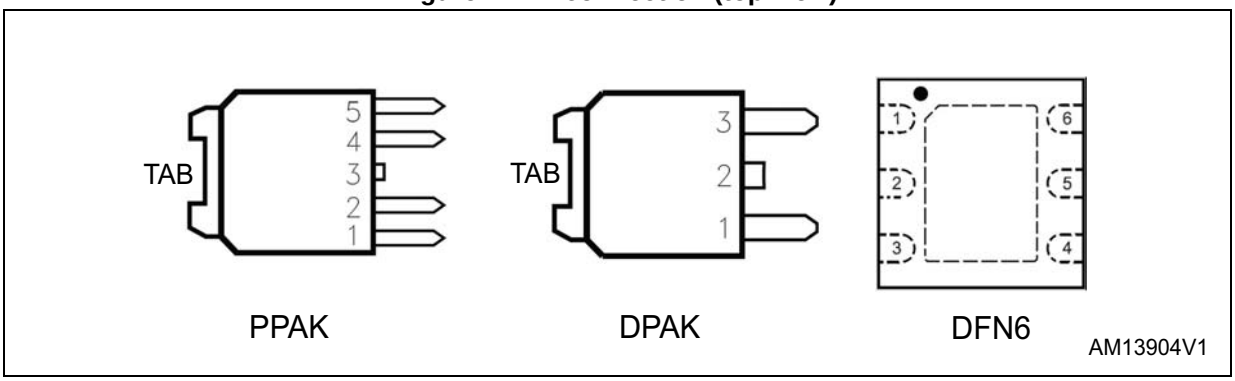


Table 1. DPAK, PPAK pin description

Pin n°		Symbol	Function
PPAK	DPAK		
5	-	ADJ/PG	For adjustable versions: error amplifier input pin For fixed versions: power-good output
2	1	V_{IN}	Input voltage
4	3	V_{OUT}	Output voltage
1	-	EN	Enable pin logic input: low = shutdown, high = active
3	2	GND	Ground
TAB	TAB	GND	Ground

Table 2. DFN6-2x2 and 3x3 pin description

Pin n°	Symbol	Function
2	ADJ/NC	For adjustable versions: error amplifier input pin For fixed versions: not connected
6	V_{IN}	Input voltage
1	V_{OUT}	Output voltage
5	EN	Enable pin logic input: low = shutdown, high = active
3	PG	Power-good output
4	GND	Ground
Exposed pad	GND	Ground

3 Typical application

Figure 3. Fixed versions

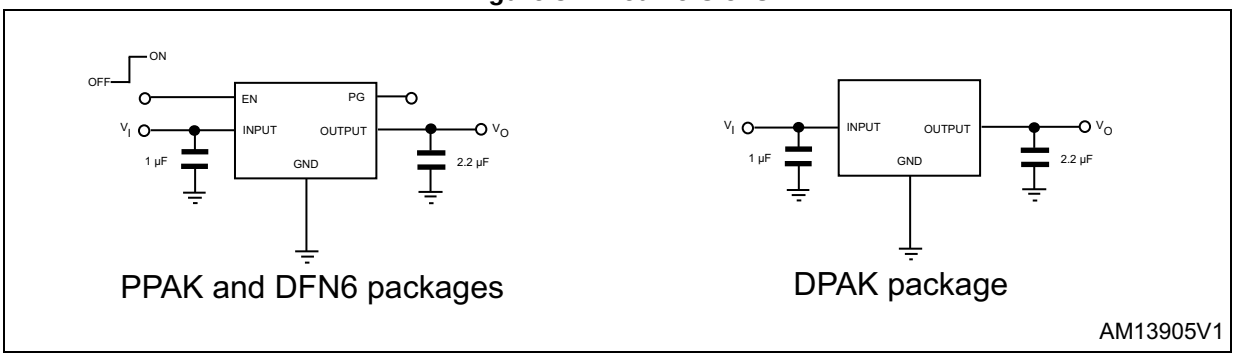
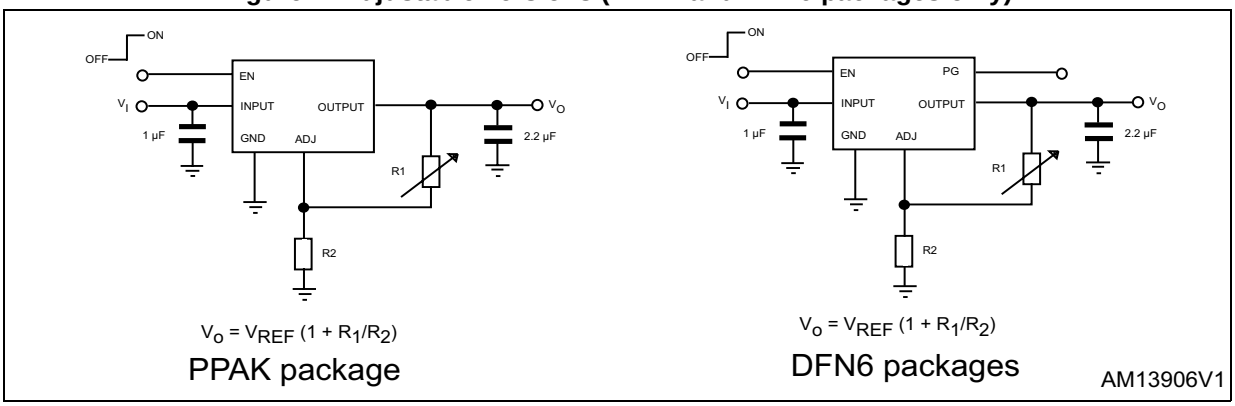


Figure 4. Adjustable versions (PPAK and DFN6 packages only)



4 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	- 0.3 to 20	V
V_{OUT}	DC output voltage	- 0.3 to V_{IN} + 0.3	V
V_{EN}	Enable input voltage	- 0.3 to V_{IN} + 0.3	V
V_{ADJ}	Adjust pin voltage	- 0.3 to 2	V
V_{PG}	PG pin voltage	- 0.3 to V_{IN} + 0.3	V
I_{LOAD}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value				Unit
		PPAK	DPAK	DFN6-2x2	DFN6-3x3	
R_{thJA}	Thermal resistance junction-ambient	100	100	65	55	°C/W
R_{thJC}	Thermal resistance junction-case	8	8	6.5	10	°C/W

5 Electrical characteristics

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V(1), C_{IN} = 1 µF, C_{OUT} = 2.2 µF, I_{LOAD} = 10 mA, V_{EN} = 2 V, unless otherwise specified.

Table 5. LDF (fixed versions) electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.6		16	V
V_{OUT}	V_{OUT} accuracy, PPAK and DFN6 versions	V_{OUT} +1 V(1)≤ V_{IN} ≤ 16 V I_{LOAD} = 10 mA	-1		1	%
		10 mA ≤ I_{LOAD} ≤ 1 A T_J = -40 to 125 °C	-1.5		1.5	%
V_{OUT}	V_{OUT} accuracy, DPAK version	V_{OUT} +1 V(1)≤ V_{IN} ≤ 16 V I_{LOAD} = 10 mA	-2		2	%
		10 mA ≤ I_{LOAD} ≤ 1 A T_J = -40 to 125 °C	-3		3	%
ΔV_{OUT}	Static line regulation	V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V		0.01		%/V
		V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V, T_J = -40 to 125 °C			0.04	
ΔV_{OUT}	Static load regulation	10 mA ≤ I_{LOAD} ≤ 1 A		0.2		%/A
		10 mA ≤ I_{LOAD} ≤ 1 A, T_J = -40 to 125 °C			0.6	
V_{DROP}	Dropout voltage (2)	I_{LOAD} = 1 A, -40 °C<T_J<125 °C		200	500	mV
I_Q	Quiescent current	ON mode: V_{EN} = 2 V I_{LOAD} = 10 mA to 1 A, T_J = -40 to 125 °C		200	800	µA
		OFF mode: V_{EN} = GND, PPAK and DFN versions		30		
		OFF mode: V_{EN} = GND, PPAK and DFN versions, -40 °C<T_J<125 °C			120	
I_{SC}	Short-circuit current	V_{IN}>3 V		1.5		A
V_{EN}	Enable input logic low	V_{IN} = 2.6 V to 16 V, -40 °C<T_J<125 °C			0.8	V
	Enable input logic high		2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		5	10	µA
PG	Power-good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power-good output voltage low	I_{SINK} = 6 mA, open drain output		0.4		

Table 5. LDF (fixed versions) electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	V_{IN} = 4.5 +/- 0.5 V_{RIPPLE} Frequency = 120 Hz, V_{OUT} = 3.3 V		60		dB
		V_{IN} = 4.5 +/- 0.5 V_{RIPPLE} Frequency = 120 Hz to 100k Hz V_{OUT} = 3.3 V		45		
e_N	Output noise voltage	Bw = 10 Hz to 100 kHz, I_{LOAD} = 100 mA C_{OUT} = 2.2 µF		45		μV_{RMS} /V_{OUT}
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			10		

1. For V_{OUT}<1.6 V; V_{IN} = 2.6 V
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.6 V

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V(1), C_{IN} = 1 µF, C_{OUT} = 2.2 µF, I_{LOAD} = 10 mA, V_{EN} = 2 V, unless otherwise specified.

Table 6. LDF (adjustable version) electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.6		16	V
V_{ADJ}	Reference voltage	V_{IN} = V_{OUT}+1 V(1)		0.8		V
	Reference voltage tolerance	V_{OUT}+1 V(1) ≤ V_{IN} ≤ 16 V I_{LOAD} = 10 mA	-1		1	%
		10 mA ≤ I_{LOAD} ≤ 1 A T_J = -40 to 125 °C	-1.5		1.5	
ΔV_{OUT}	Static line regulation	V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V		0.01		%/V
		V_{OUT}+1V(1)≤ V_{IN} ≤ 16 V, T_J = -40 to 125 °C			0.04	
ΔV_{OUT}	Static load regulation	10 mA ≤ I_{LOAD} ≤ 1 A		0.2		%/A
		10 mA ≤ I_{LOAD} ≤ 1 A, T_J = -40 to 125 °C		0.2	0.6	
V_{DROP}	Dropout voltage(2)	V_{OUT} fixed to 2.5 V, I_{LOAD} = 1 A, -40 °C<T_J<125 °C		200	500	mV
I_Q	Quiescent current	ON mode: V_{EN} = 2 V I_{LOAD} = 10 mA to 1 A, T_J = -40 to 125 °C		200	800	µA
		OFF mode: V_{EN} = GND, PPAK and DFN versions		30		
		OFF mode: V_{EN} = GND, PPAK and DFN versions, -40 °C<T_J<125 °C			120	
I_{SC}	Short-circuit current	V_{IN}>3 V		1.5		A
V_{EN}	Enable input logic low	V_{IN} = 2.6 V to 16 V, -40 °C<T_J<125 °C			0.8	V
	Enable input logic high		2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		5	10	µA
PG	Power-good output threshold	Rising edge		0.92* V_{ADJ}		V
		Falling edge		0.8* V_{ADJ}		
	Power-good output voltage low	I_{SINK} = 6 mA, open drain output		0.4		
SVR	Supply voltage rejection	V_{IN} = 3 V +/- 0.5 V_{RIPPLE} Frequency= 120 Hz, V_{OUT} = 0.8 V		62		dB
		V_{IN} = 3 V +/- 0.5 V_{RIPPLE} Frequency = 120 Hz to 100 kHz, V_{OUT} = 0.8V		55		

Table 6. LDF (adjustable version) electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
e_N	Output noise voltage	B_w = 10 Hz to 100 kHz, I_{LOAD} = 100 mA C_{OUT} = 2.2 µF		50		μV_{RMS} /V_{OUT}
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			10		

1. For V_{OUT}<1.6 V; V_{IN} = 2.6 V
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply to output voltages below 1.6 V

6 Application information

6.1 External capacitors

The LDF voltage regulator requires external ceramic capacitors to assure the control loop stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance (see *figures 25, 26*). Input/output capacitors should be located as closer as possible to the relative pins.

6.1.1 Input capacitor

An input capacitor, whose minimum value is 1 µF, must not be located farther than 0.5" from the input pin of the device and returned to a clean analog ground.

6.1.2 Output capacitor

Ceramic capacitors could be used on the output, provided that they must meet the minimum amount of capacitance and E.S.R. (equivalent series resistance) value required. 2.2 µF is suggested as minimum capacitance to guarantee the stability of the regulator. Anyway, other C_{OUT} values can be used according to the *figures 25, 26* showing the allowable ESR range as a function of the output capacitance.

The output capacitor must maintain its ESR in the stable region over the full operating temperature range to assure stability. Besides, capacitor tolerance and temperature variation must be taken into account to assure the minimum amount of capacitance.

6.2 Enable pin operation

This pin can be used to turn OFF the regulator when it is pulled down, so to drastically reduce the current consumption. When the enable feature is not used, this pin must be tied to V_{IN} to keep the regulator output in ON state every time. To assure the proper operation, the signal source, used to drive the EN pin, must be able to swing above and below the specified thresholds listed in the electrical characteristics (V_{EN}). The EN pin must not be left floating because it is not internally pulled down/up.

6.3 Power Good

The LDF features an open drain PG pin to sequence either external supplies or loads and to provide fault detection. This pin requires an external resistor (R_{PG}) to pull Power Good high when the output is within the power-good tolerance window. Typical values for this resistor range from 10 kΩ to 100 kΩ.

7 Typical characteristics

$C_{IN} = C_{OUT} = 1$ µF, $V_{IN} = V_{OUT} + 1$ V, V_{EN} to V_{IN}, $I_{OUT} = 10$ mA, unless otherwise specified.

Figure 5. Output voltage vs. temperature, fixed version

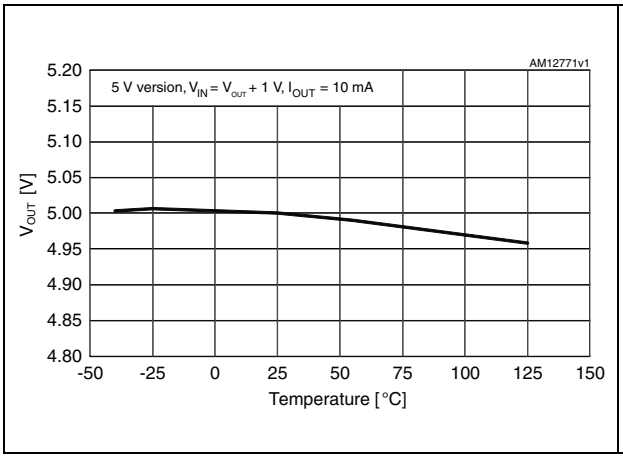


Figure 6. Output voltage vs. temperature, adjustable version

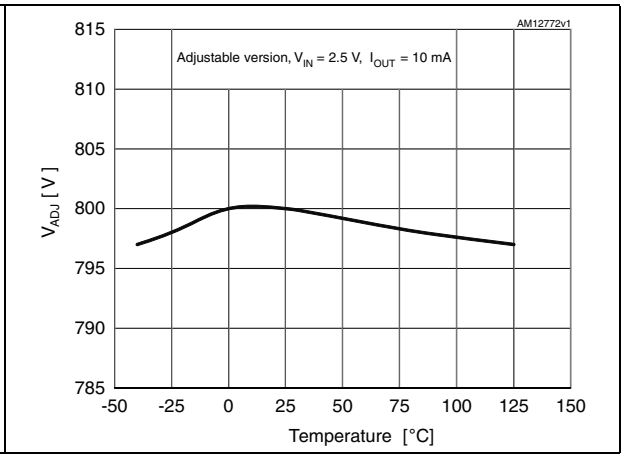


Figure 7. Line regulation vs. temperature

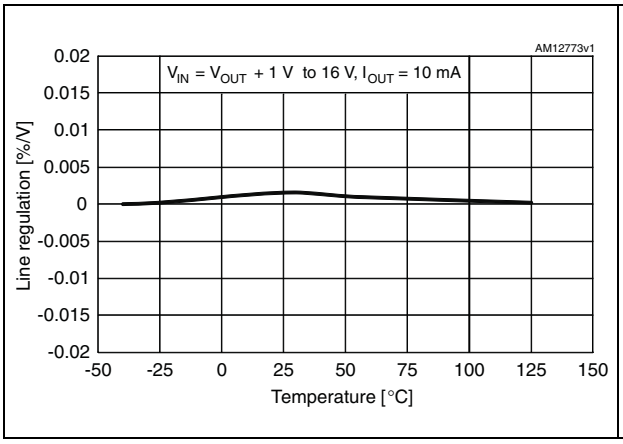


Figure 8. Load regulation vs. temperature

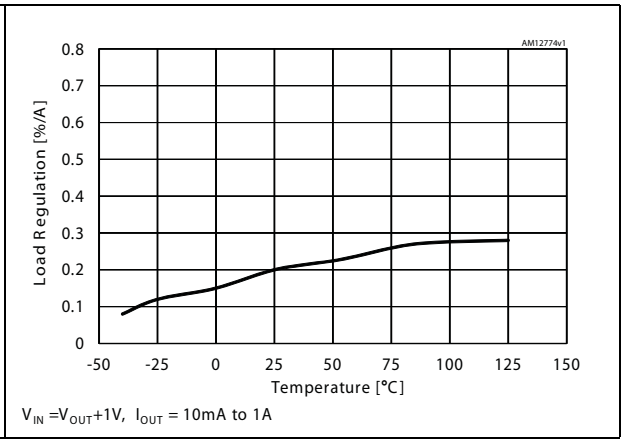


Figure 9. Short-circuit current vs. dropout

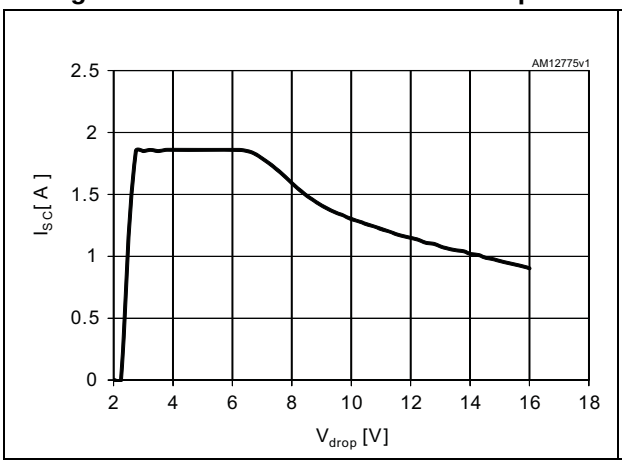


Figure 10. Dropout voltage vs. temperature

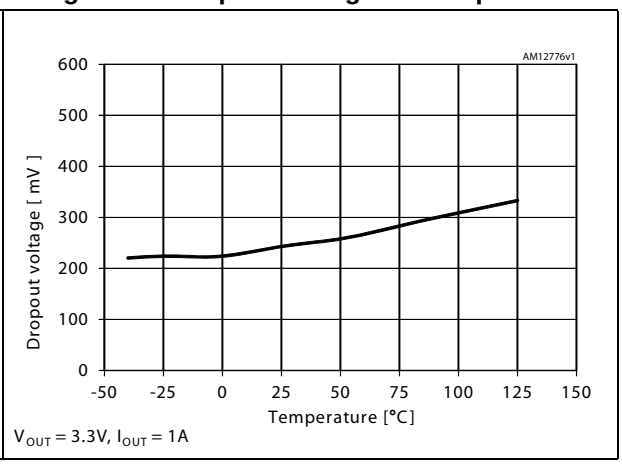


Figure 11. Quiescent current vs. temperature, I_{OUT} = 10 mA

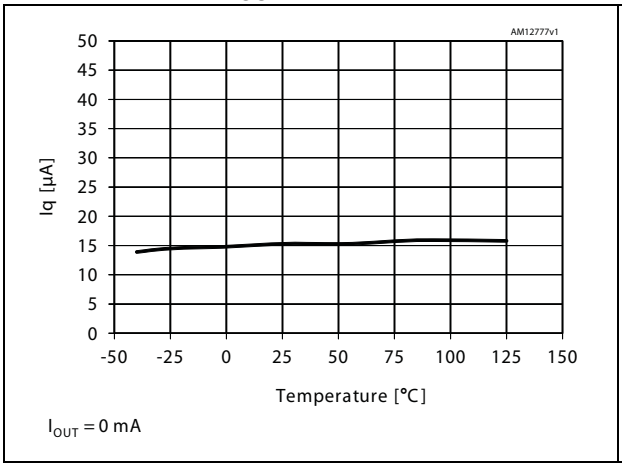


Figure 12. Quiescent current vs. temperature, I_{OUT} = 1 A

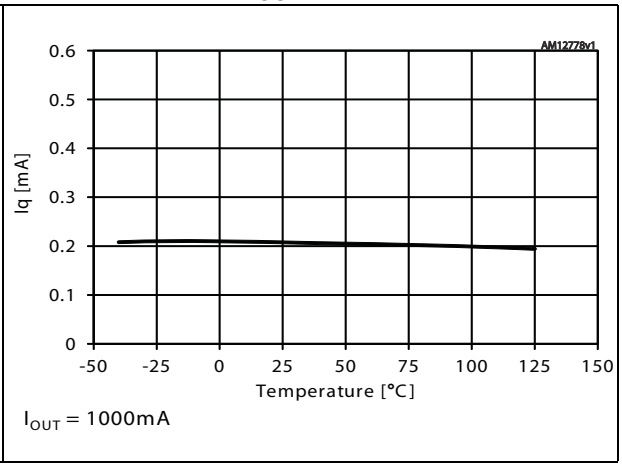


Figure 13. Shutdown current vs. temperature

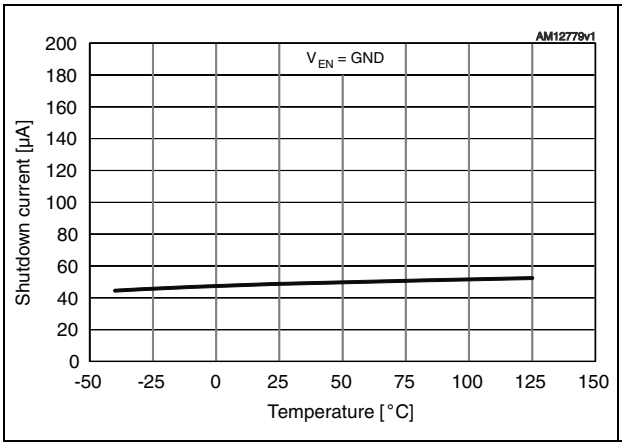


Figure 14. Enable pin current vs. temperature

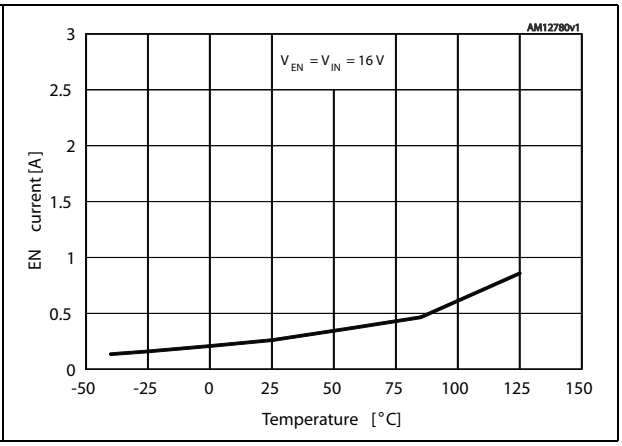


Figure 15. Enable high threshold vs. temperature

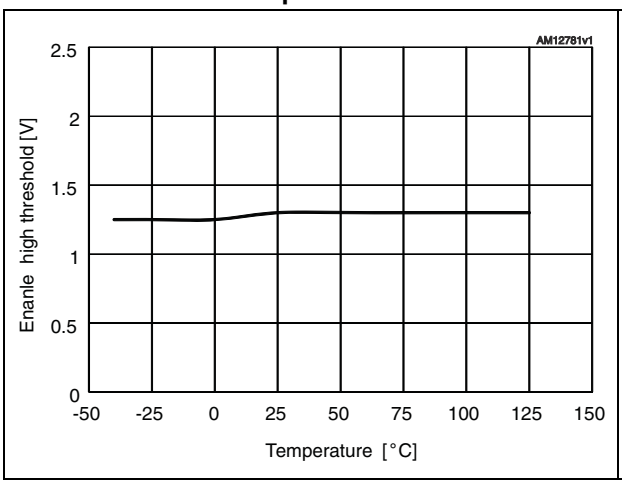


Figure 16. Enable low threshold vs. temperature

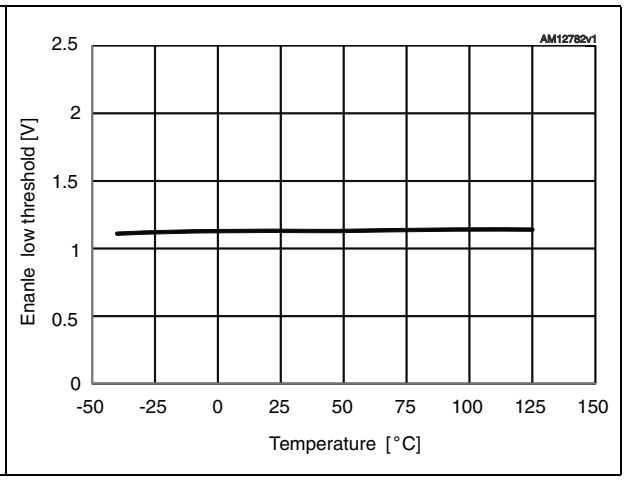


Figure 17. Output voltage vs. input voltage

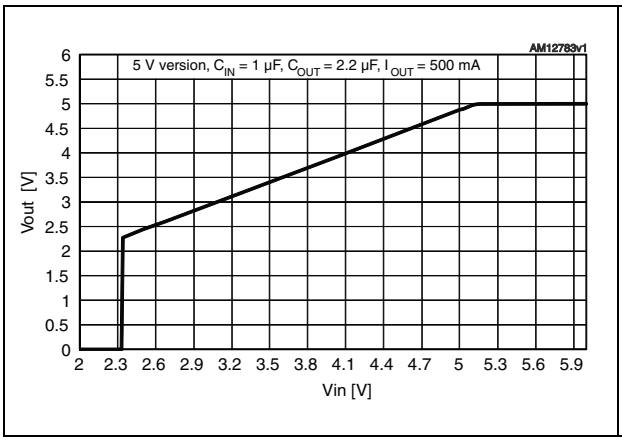


Figure 18. Line transient

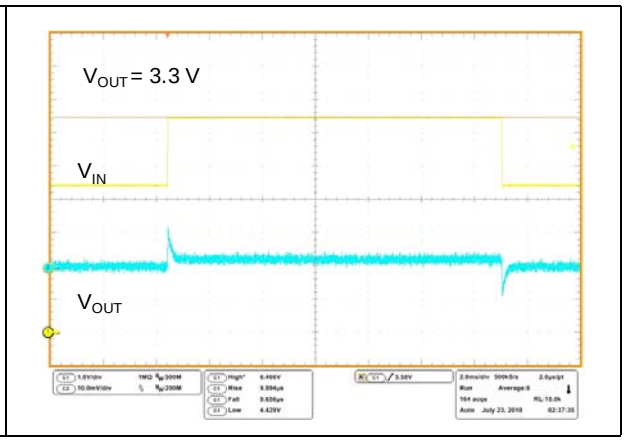
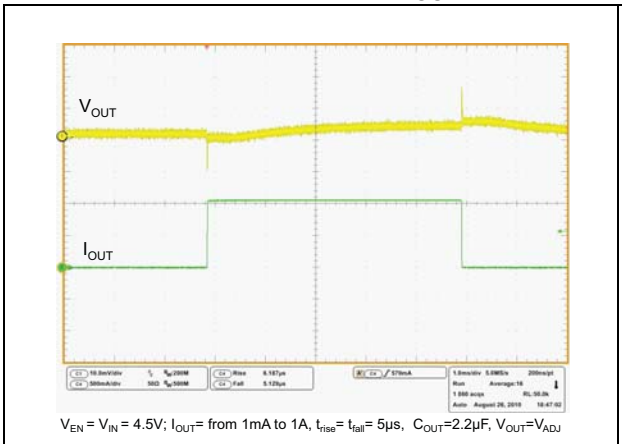
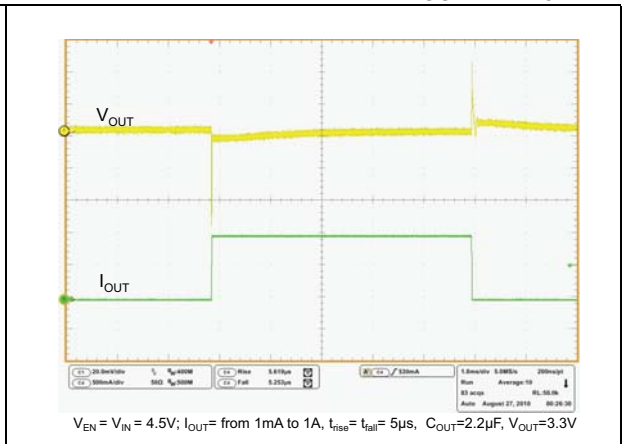


Figure 19. Load transient (V_{OUT} = 3.3 V)



$V_{EN} = V_{IN} = 4.5V$; I_{OUT}= from 1mA to 1A, $t_{rise} = t_{fall}$= 5µs, C_{OUT}=2.2µF, $V_{OUT}=V_{ADJ}$

Figure 20. Load transient ($V_{OUT} = V_{ADJ}$)



$V_{EN} = V_{IN} = 4.5V$; I_{OUT}= from 1mA to 1A, $t_{rise} = t_{fall}$= 5µs, C_{OUT}=2.2µF, V_{OUT}=3.3V

Figure 21. Start-up transient

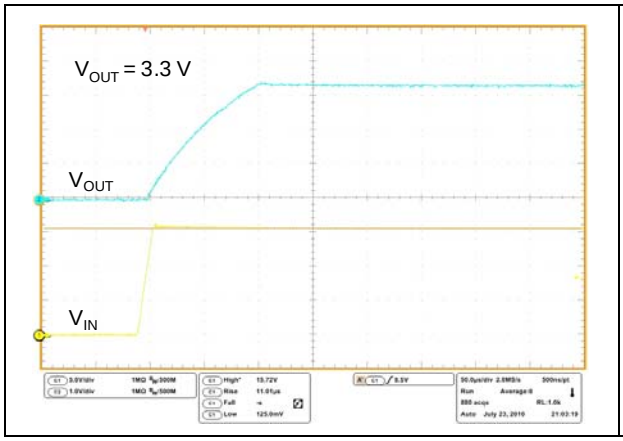


Figure 22. Enable transient

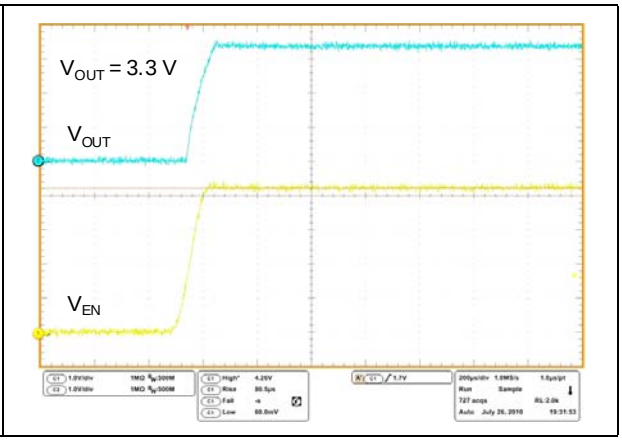


Figure 23. SVR vs. frequency (V_{OUT} = 5 V)

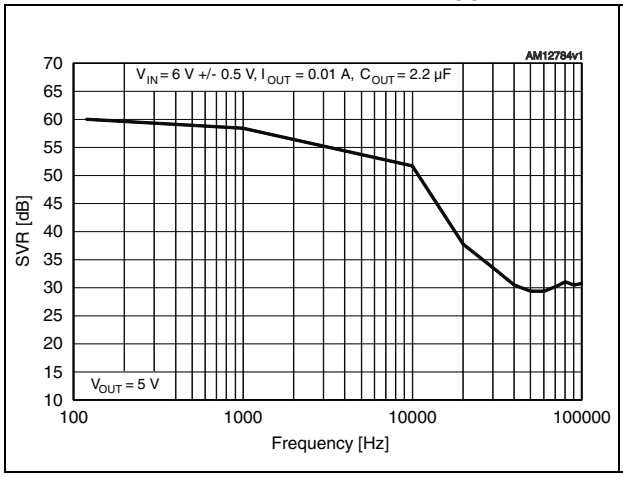


Figure 24. SVR vs. frequency (V_{OUT} = V_{ADJ})

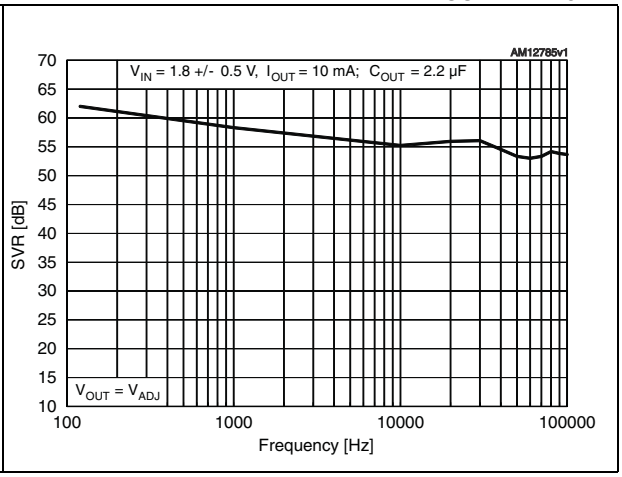


Figure 25. Stability plane ADJ (C_{OUT}, ESR)

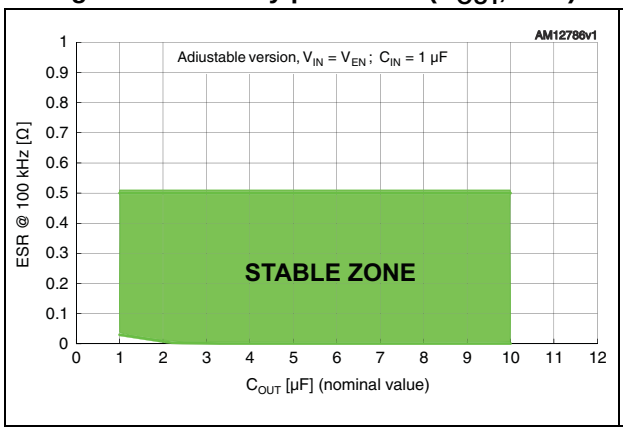
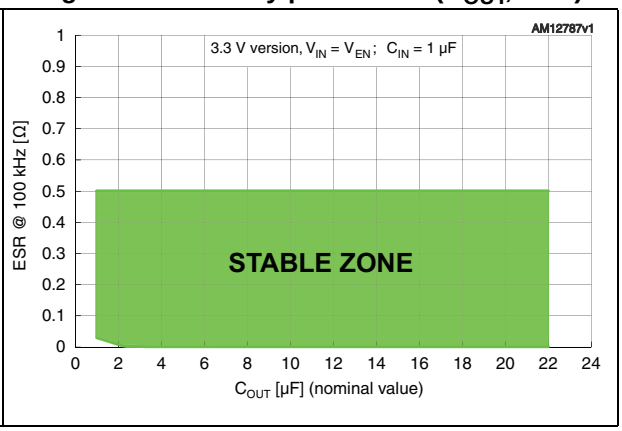


Figure 26. Stability plane 3.3 V (C_{OUT}, ESR)



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 7. DPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 27. DPAK drawings

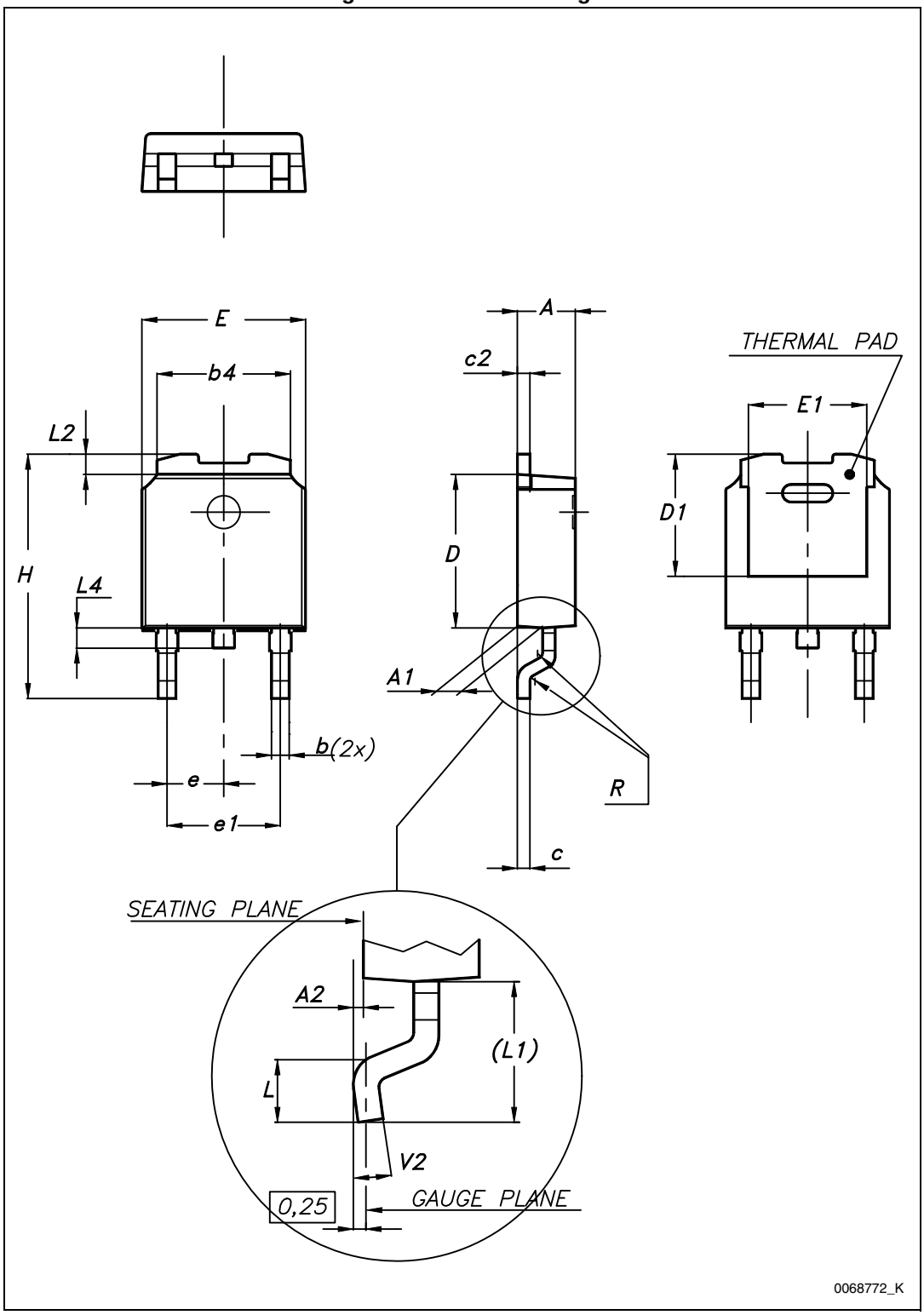
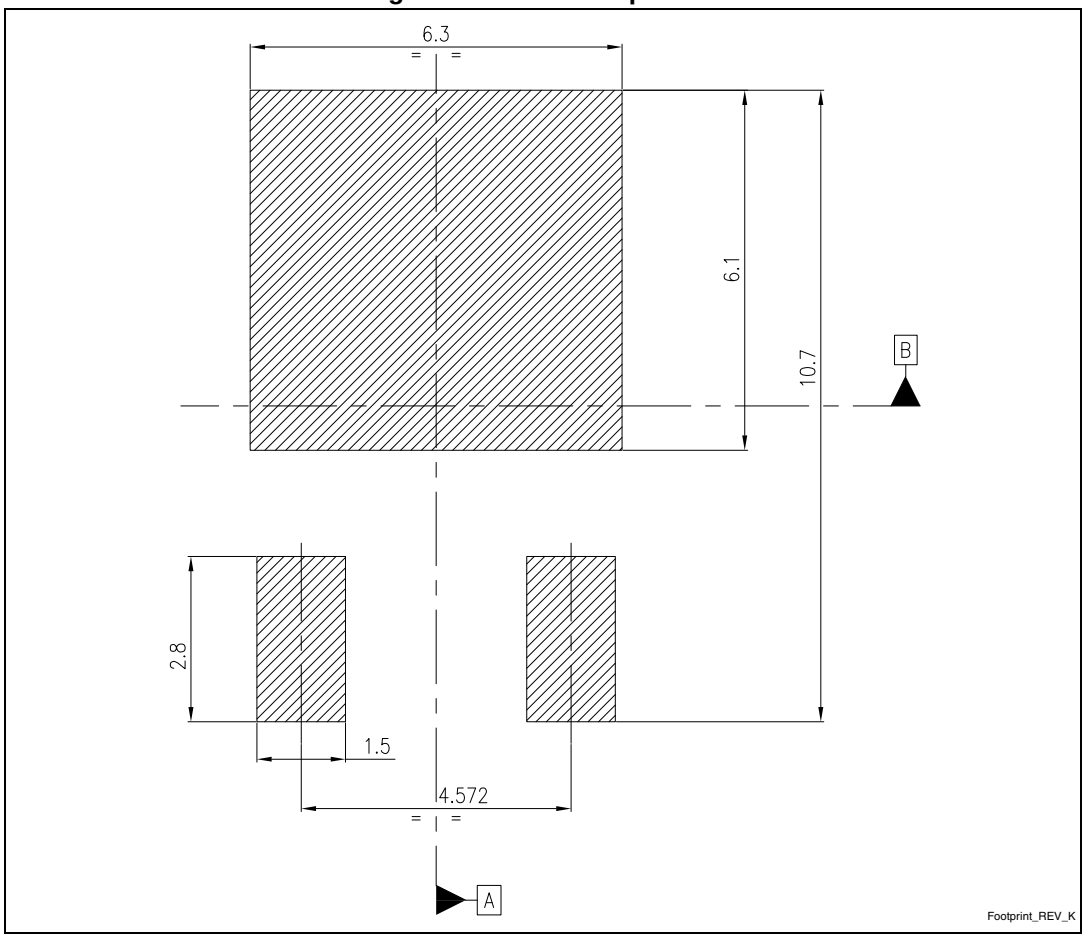


Figure 28. DPAK footprint [(a)]



a. All dimensions are in millimeters.

Table 8. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

Figure 29. PPAK drawings

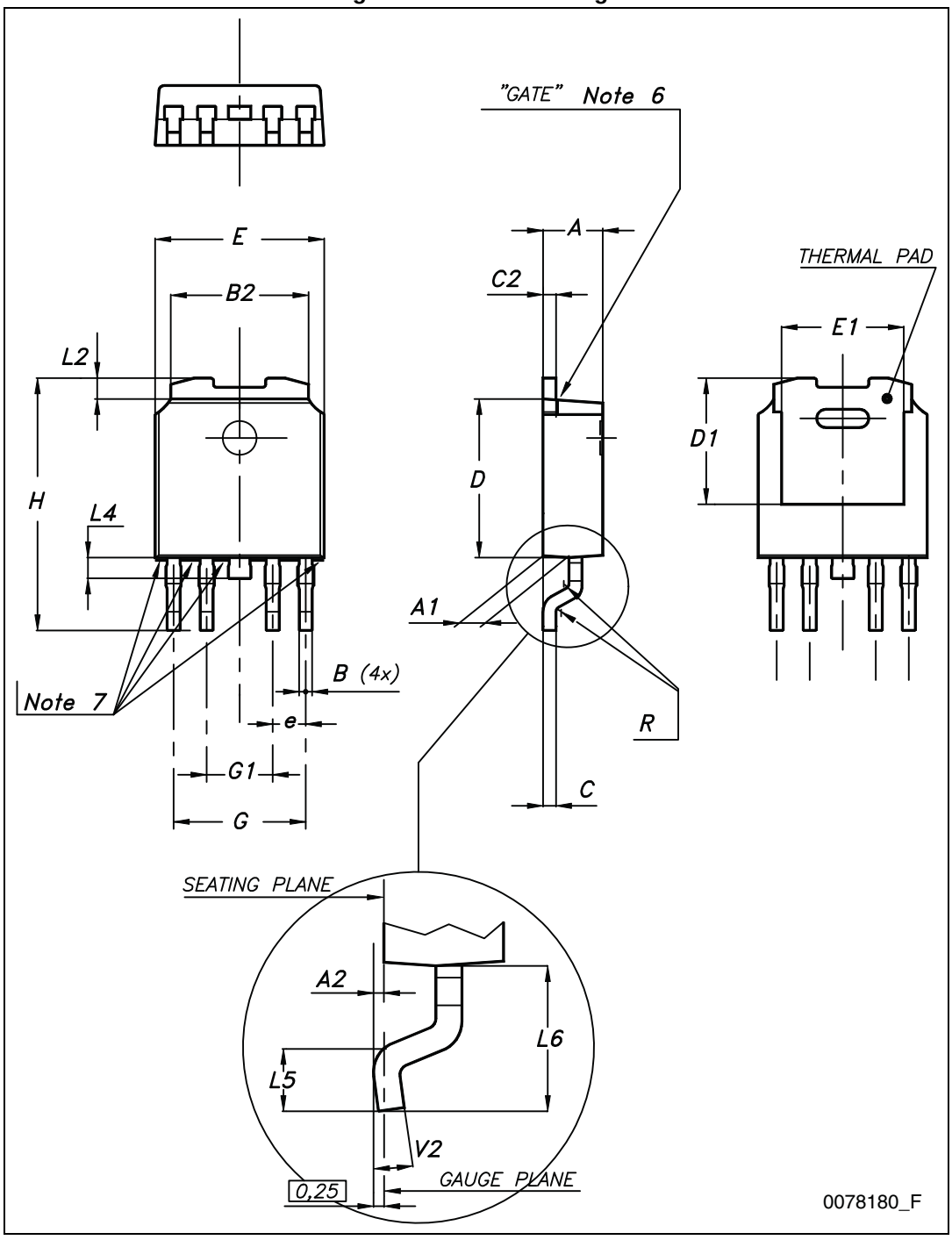


Table 9. DFN6-3x3 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 30. DFN6-3x3 drawings

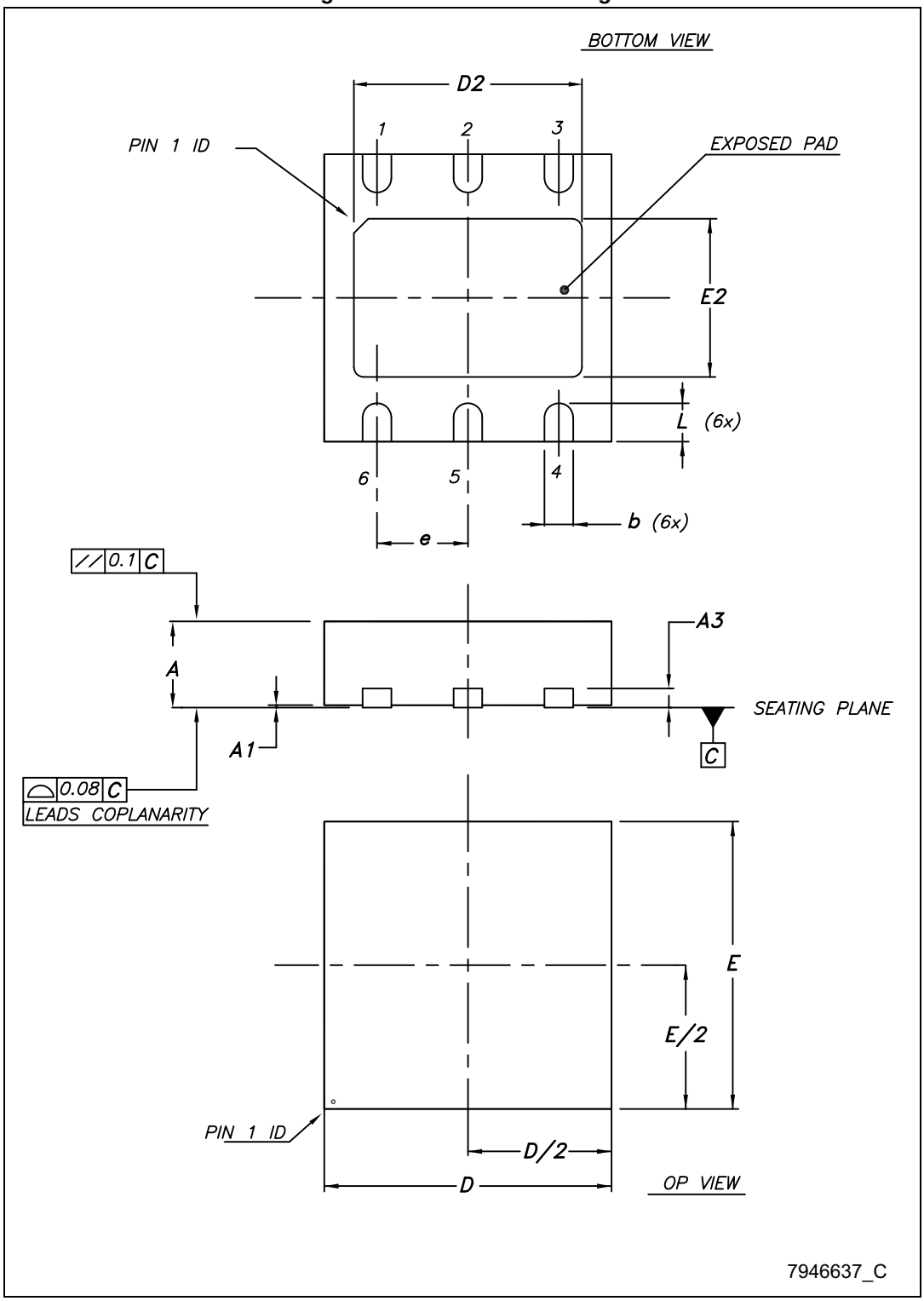


Figure 31. DFN6-3x3 footprint

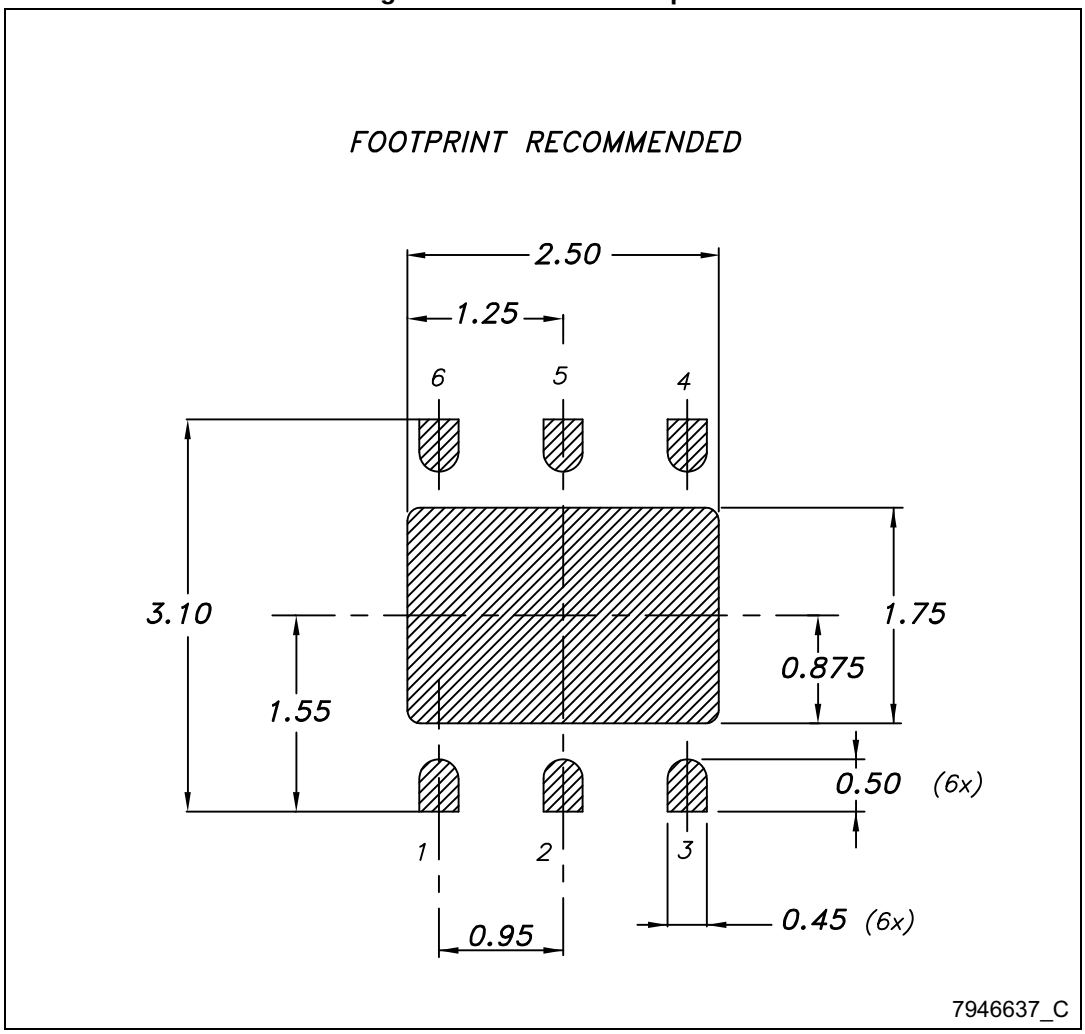


Table 10.DFN6-2x2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D	2.00 BSC		
E	2.00 BSC		
e	0.65 BSC		
D2	1.45	1.60	1.70
E2	0.85	1.00	1.10
L	0.20	0.25	0.30
K	0.15		
aaa	0.05		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N	6		

Figure 32. DFN6-2x2 drawings

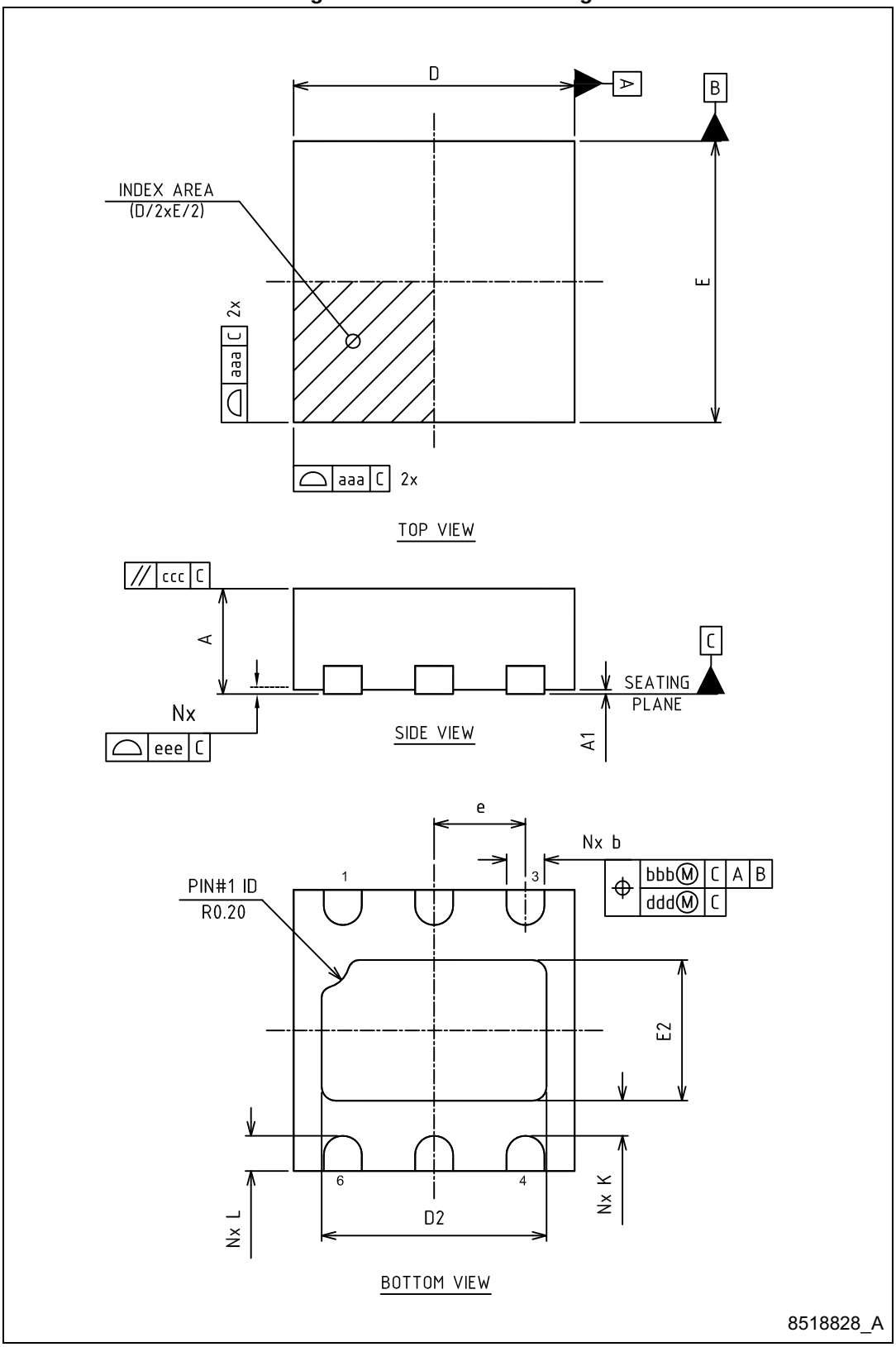
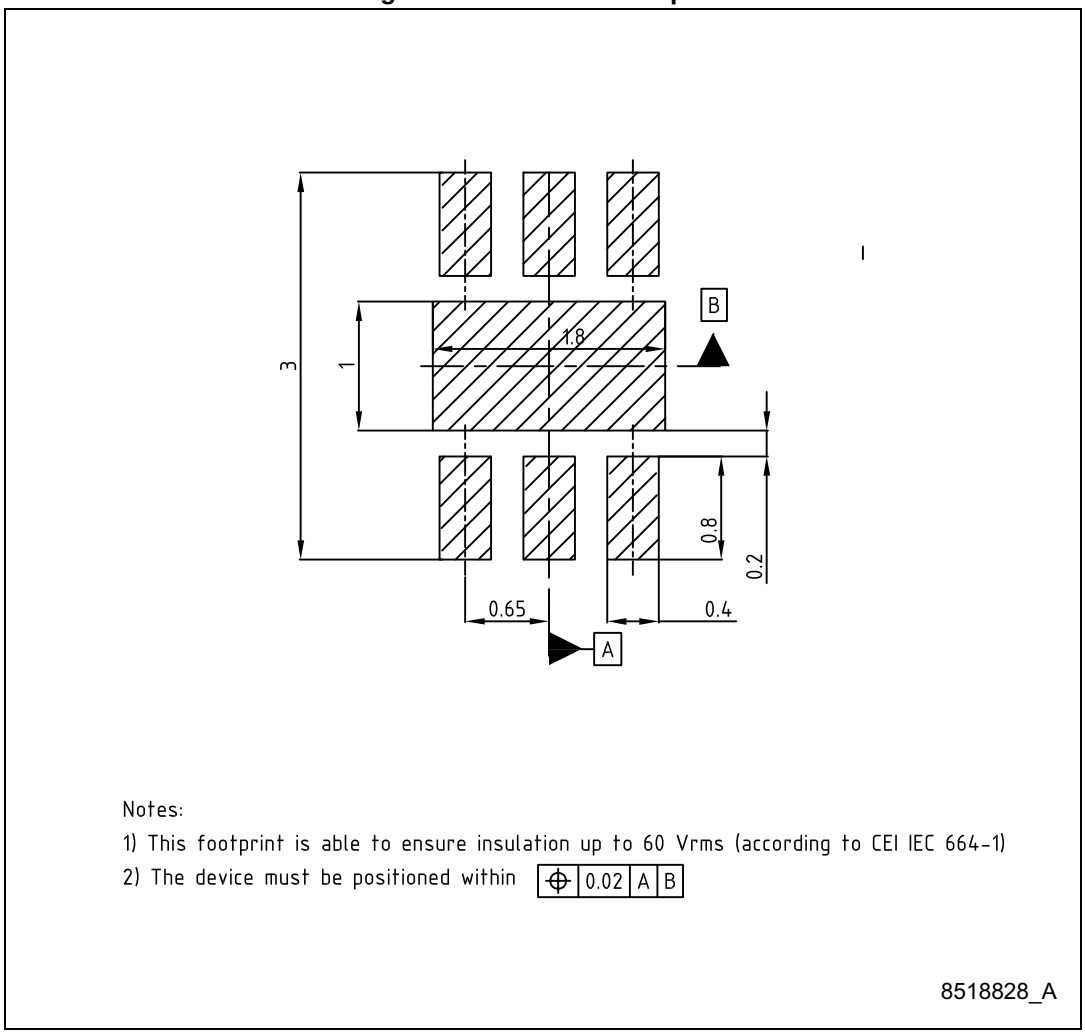


Figure 33. DFN6-2x2 footprint



9 Packaging mechanical data

Table 11. PPAK and DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 34. PPAK and DPAK tape

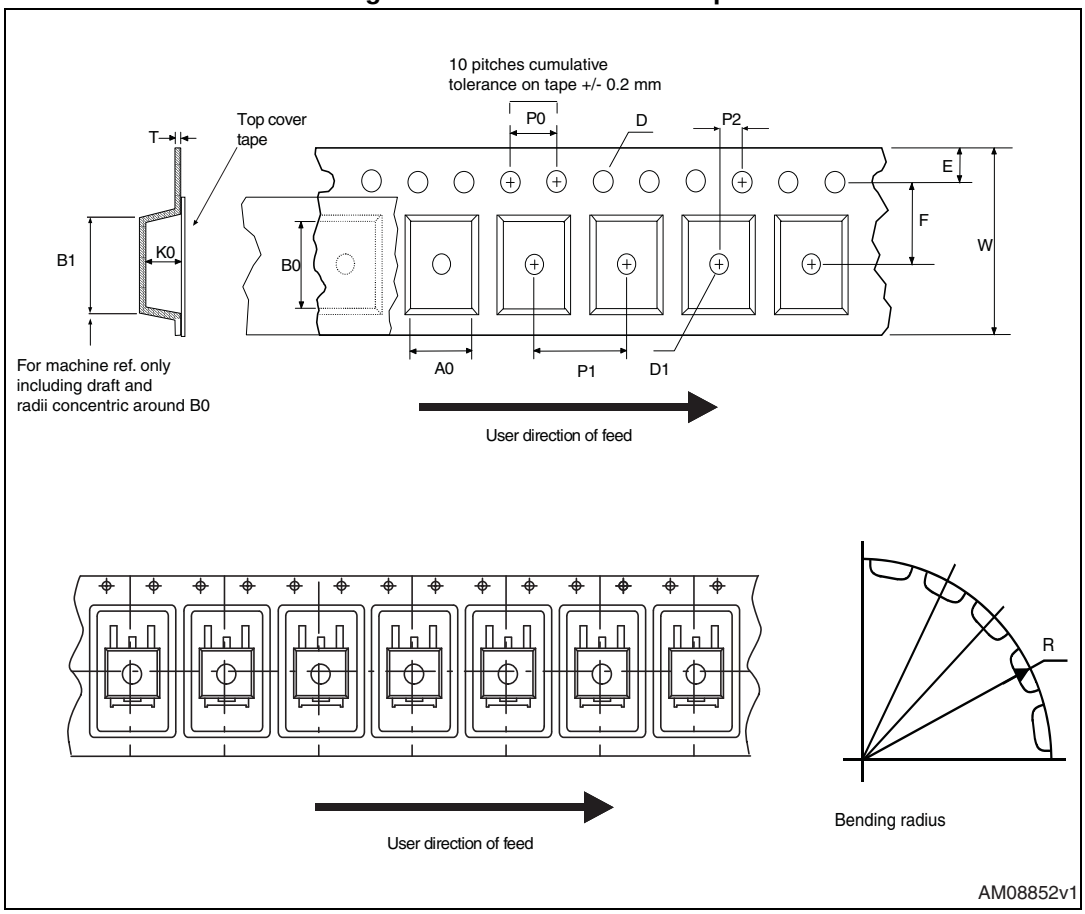


Figure 35. PPAK and DPAK reel

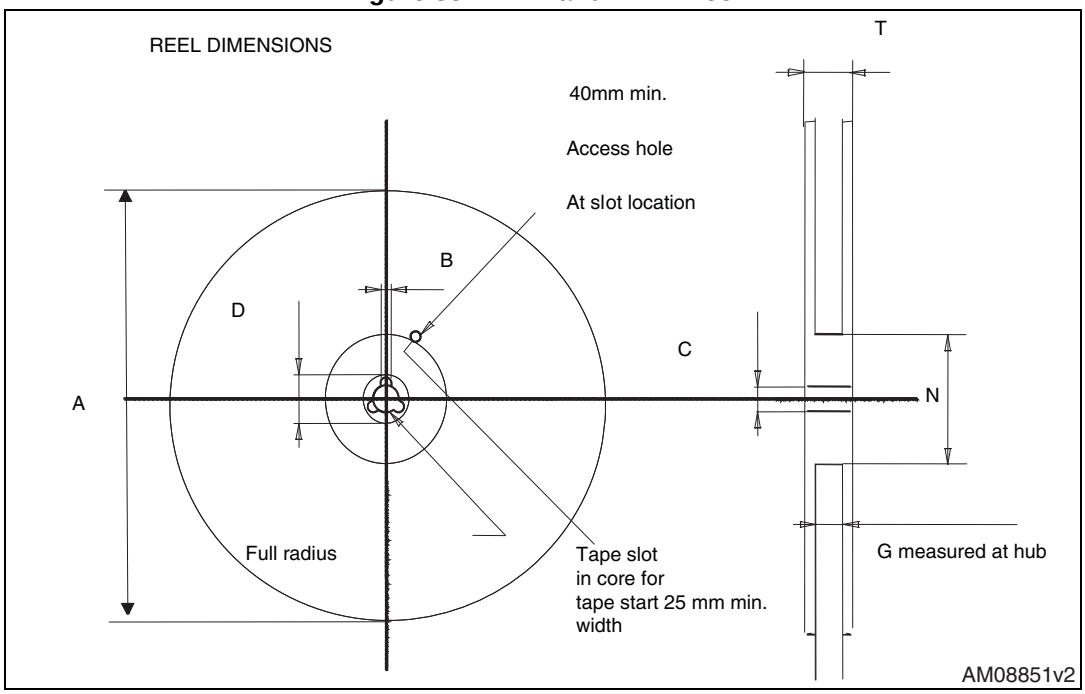


Table 12. DFN6-3x3 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

Figure 36. DFN6-3x3 tape

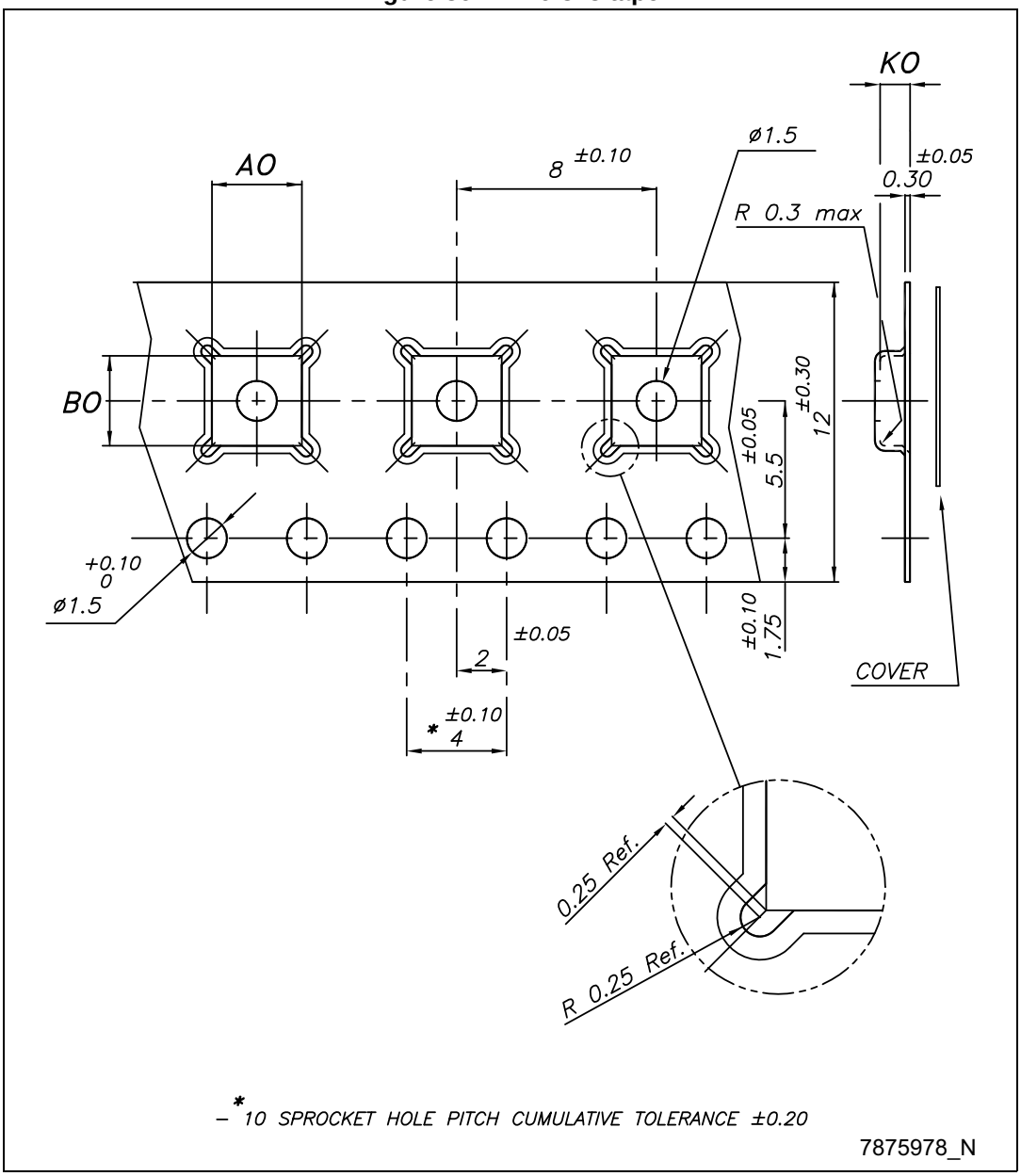


Figure 37. DFN6-3x3 reel

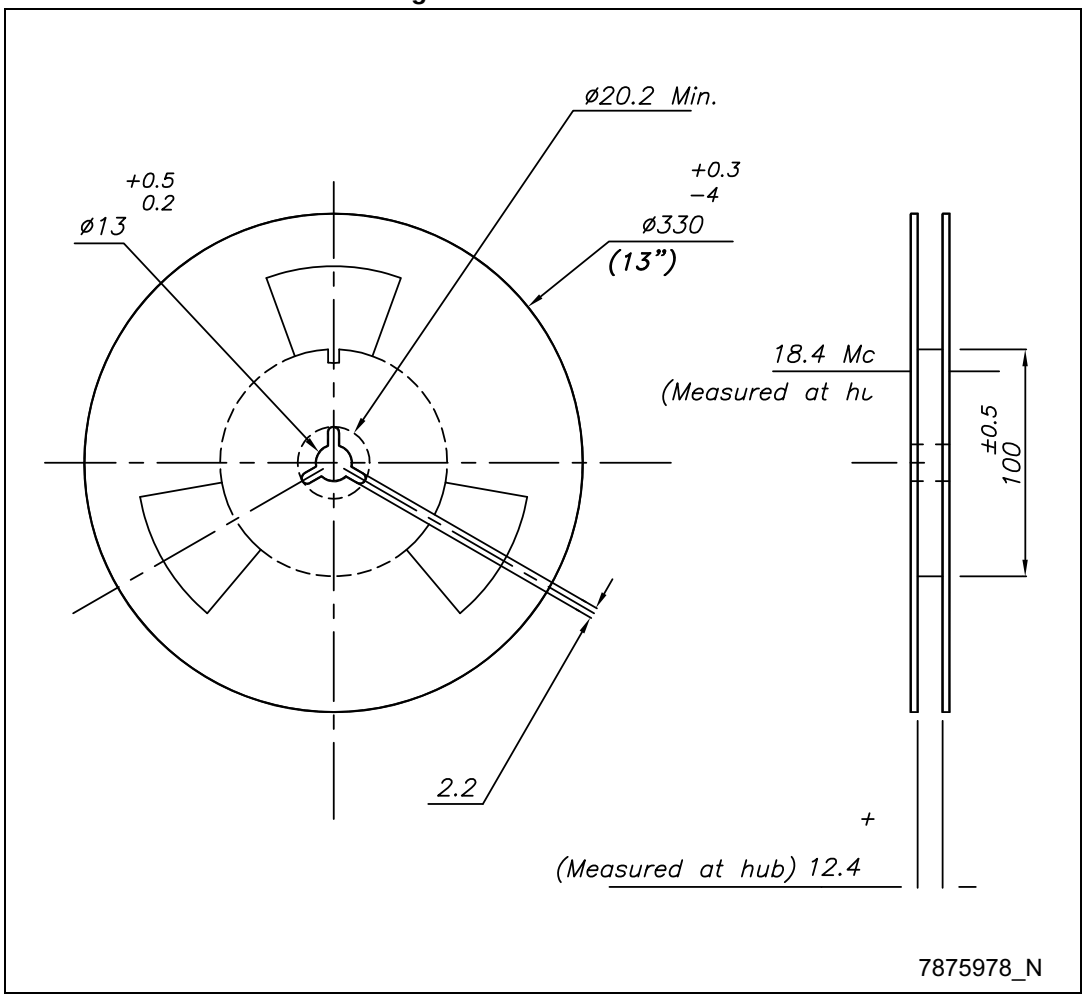
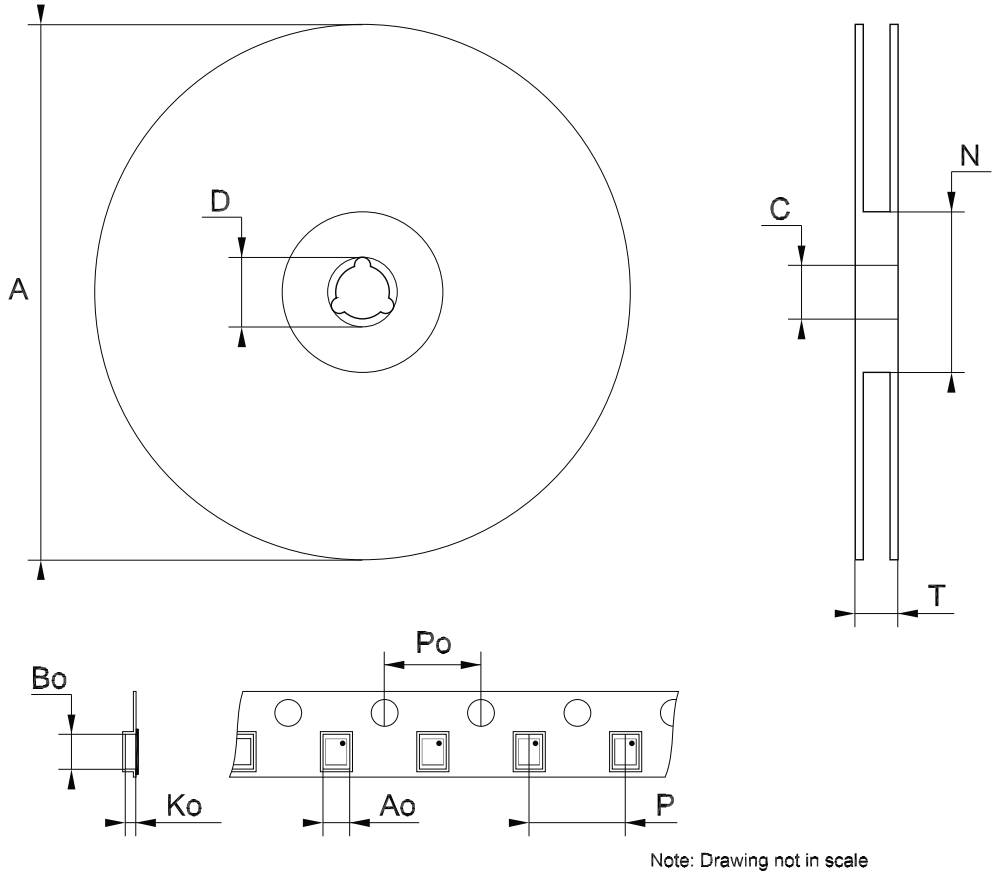


Table 13. DFN6-2x2 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8		13.2
D	20.2		
N	60		
T			14.4
Ao		2.4	
Bo		2.4	
Ko		1.3	
Po		4	
P		4	

Figure 38. DFN6-2x2 tape and reel



10 Order codes

Different output voltage versions of the LDF available on request:

Table 14. Device summary

Packages				Output voltages
PPAK	DPAK	DFN6-3x3	DFN6-2x2	
LDF18PT-TR				1.8 V
LDF25PT-TR				2.5 V
LDF33PT-TR	LDF33DT-TR			3.3 V
LDFPT-TR		LDFPUR	LDFPVR	ADJ

11 Revision history

Table 15. Document revision history

Date	Revision	Changes
05-Dec-2013	1	Initial release.

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