Ordering number : EN5505D

SANYO Semiconductors
DATA SHEET

Monolithic Digital IC

LB1845 — PWM Current Controlling Stepping Motor Driver

Overview

The LB1845 is a PWM current control type stepping motor driver that uses a bipolar drive scheme. It is particularly suitable for driving carriage and paper feed stepping motors in printers and similar products.

Features

- PWM current control (fixed off time scheme)
- Digital load current selection function
- Sustained output voltage: 45V
- Built-in thermal shutdown circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V_{BB} max		45	V
Peak output current	I_O peak	tW ≤ 20μs	1.75	A
Continuous output current	I_O max		1.5	A
Logic block supply voltage	V_{CC}		7.0	V
Logic input voltage range	V_{IN}		-0.3 to V_{CC}	V
Emitter output voltage	V_E		1.0	V
Allowable power dissipation	Pd max1	Independent IC	3.0	W
	Pd max2	With an arbitrarily large heat sink	20.0	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

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Recommended Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V_{BB}		10 to 44.5	V
Logic block supply voltage	V_{CC}		4.75 to 5.25	V
Reference voltage	V_{REF}		1.5 to 7.5	V

Electrical Characteristics at Ta = 25°C, V_{BB} = 38V, V_{CC} = 5V, V_{REF} = 5V

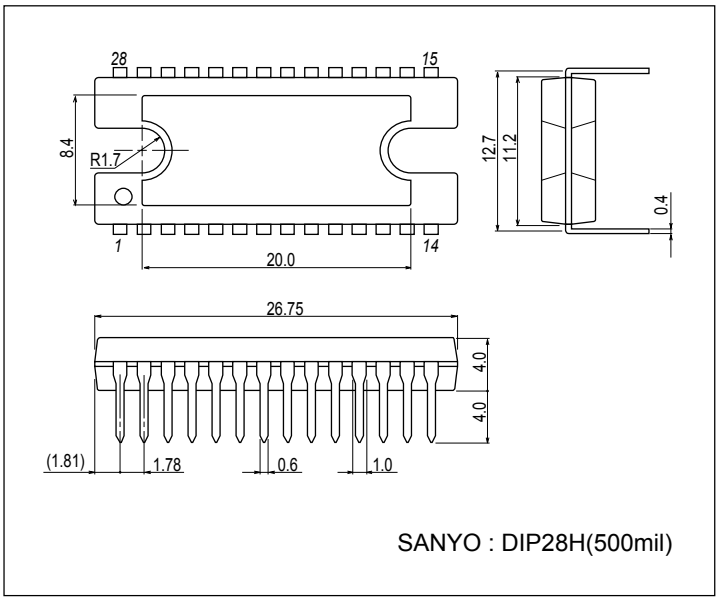
Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
[Output Block]						
Output stage supply current	I_{BB} ON			12	16	mA
	I_{BB} OFF			0.7	0.9	
Output saturation voltage 1	V_O(sat)1	I_O = +1.0A Sink		1.2	1.4	V
	V_O(sat)2	I_O = +1.5A Sink		1.4	1.7	
	V_O(sat)3	I_O = -1.0A Source		1.1	1.3	
	V_O(sat)4	I_O = -1.5A Source		1.3	1.6	
Output leakage current	I_O(leak)1	V_O = V_{BB} Sink			50	μA
	I_O(leak)2	V_O = 0V Source	-50			
Sustained output voltage	V(sus)	*	45			V
[Logic Block]						
Logic supply current	I_{CC} ON	I_0 = 0.8V, I_1 = 0.8V		19.5	25.3	mA
	I_{CC} OFF	I_0 = 2.4V, I_1 = 2.4V		15.5	20.1	
Input voltage	V_{IH}		2.4			V
	V_{IL}				0.8	
Input current	I_{IH}	V_{IH} = 2.4V			10	μA
	I_{IL}	V_{IL} = 0.8V	-10			
Current control threshold voltage	V_{REF}/V_{SENSE}	I_0 = 0.8V, I_1 = 0.8V	9.5	10	10.5	
		I_0 = 2.4V, I_1 = 0.8V	13.5	15	16.5	
		I_0 = 0.8V, I_1 = 2.4V	25.5	30	34.5	
Thermal shutdown temperature	T_S			170		°C

* Note: Design guaranteed value.

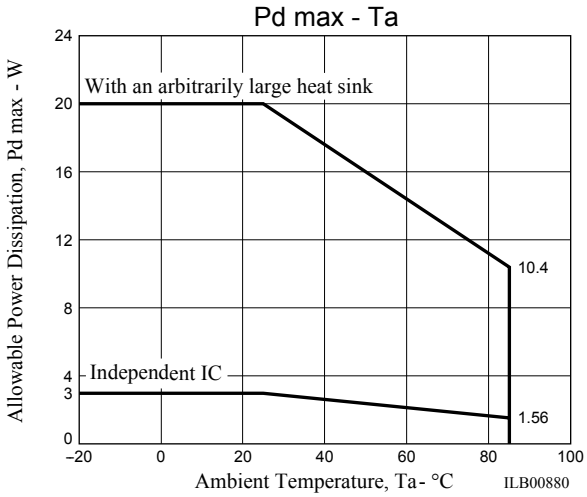
Package Dimensions

unit: mm (typ)

3147C



SANYO : DIP28H(500mil)



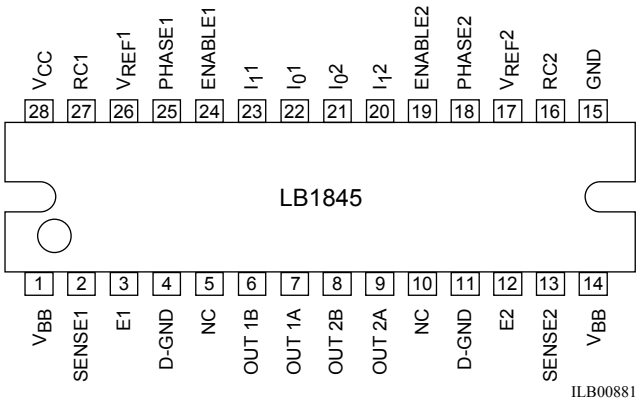
Truth Table

ENABLE	PHASE	OUTA	OUTB
L	H	H	L
L	L	L	H
H	-	OFF	OFF

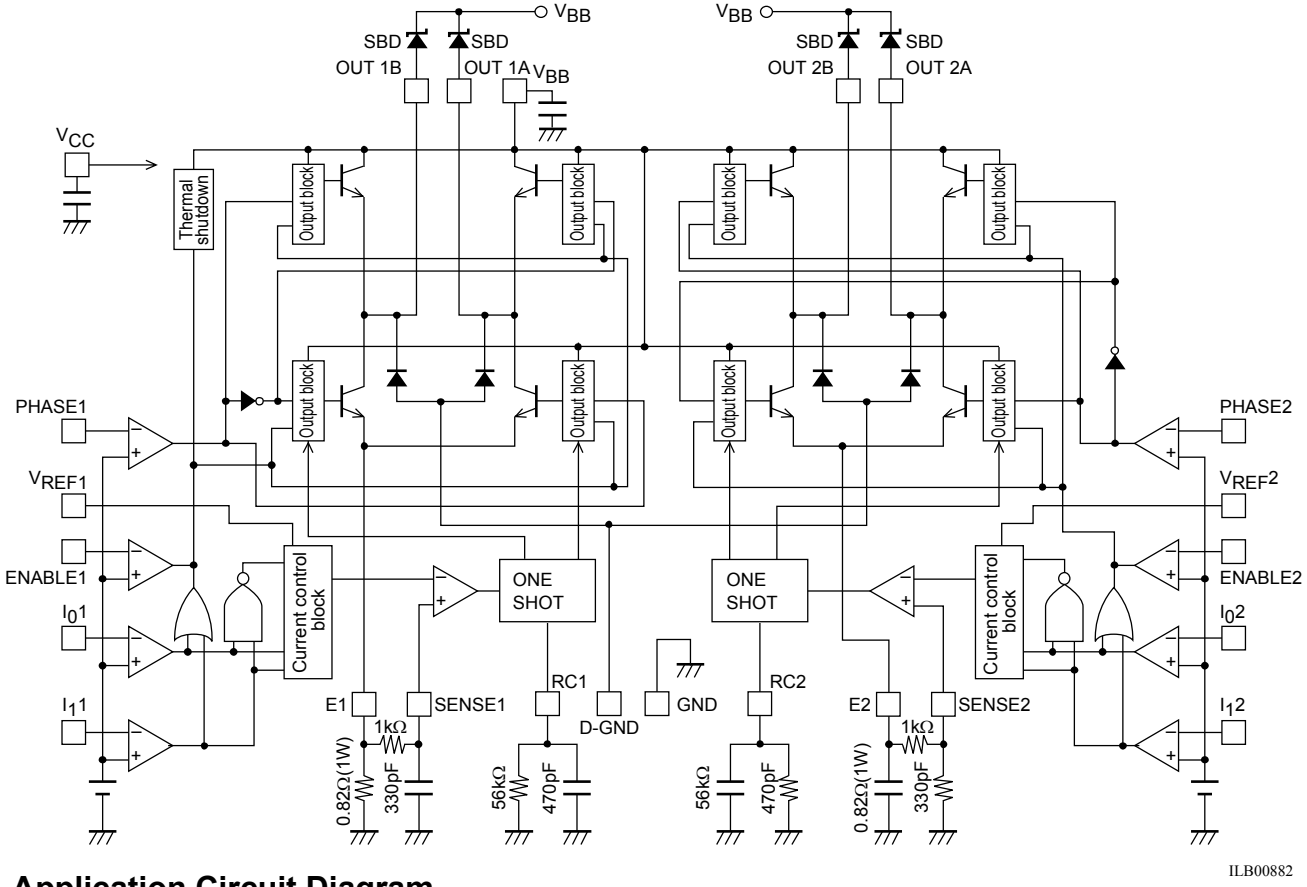
I_0	I_1	Output Current
L	L	$V_{REF}/(10\times R_E) = I_{OUT}$
H	L	$V_{REF}/(15\times R_E) = I_{OUT}\times 2/3$
L	H	$V_{REF}/(30\times R_E) = I_{OUT}\times 1/3$
H	H	0

Note: Outputs is OFF when ENABLE is high or in the $I_0 = I_1$ = high state.

Pin Assignment



Block Diagram



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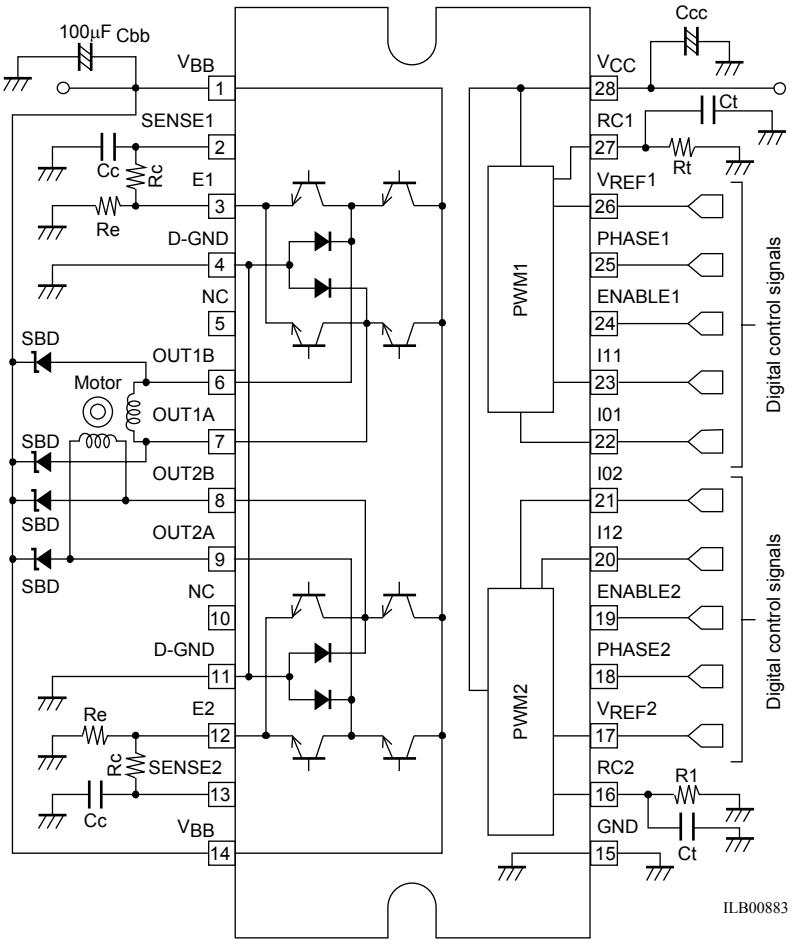
Application Circuit Diagram



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Off time setting values toff≈CtRt

Re=0.82Ω(1W)
V_{REF}=5V
Rt=56kΩ
Ct=470pF
Rc=1kΩ
Cc=330pF
Cbb=100μF

Pin Description

Pin No	Pin	Function
1, 14	V_{BB}	Output stage power-supply voltage
2 13	SENSE1 SENSE2	Set current detection pins. Connect these pins, fed back through noise filters, to E1 and E2.
3 12	E1 E2	The set current is controlled by the resistors Re inserted between these pins and ground.
4, 11	D-GND	Internal diode anode connection
6 7 8 9	OUT1B OUT1A OUT2B OUT2A	Outputs
15	GND	Ground
27 16	RC1 RC2	Used to set the output off time for the switched output signal. The fixed off times are set by the capacitors and resistors connected to these pins. toff = CR.
26 17	$V_{REF}1$ $V_{REF}2$	Output current settings The output current is determined by the voltage (in the range 1.5 to 7.5V) input to these pins.
25 18	PHASE1 PHASE2	Output phase switching inputs. High-level input: OUTA = high, OUTB = low Low-level input: OUTA = low, OUTB = high
24 19	ENABLE1 ENABLE2	Output on/off settings High-level input: output off Low-level input: output on
22, 23 21, 20	$I_0$1, $I_1$1 $I_0$2, $I_1$2	Digital inputs that set the output current The output currents can be set to 1/3, 2/3, or full by setting these pins to appropriate combinations of high and low levels.
28	V_{CC}	Logic block power supply

Timing chart for pin switching operations during PWM drive

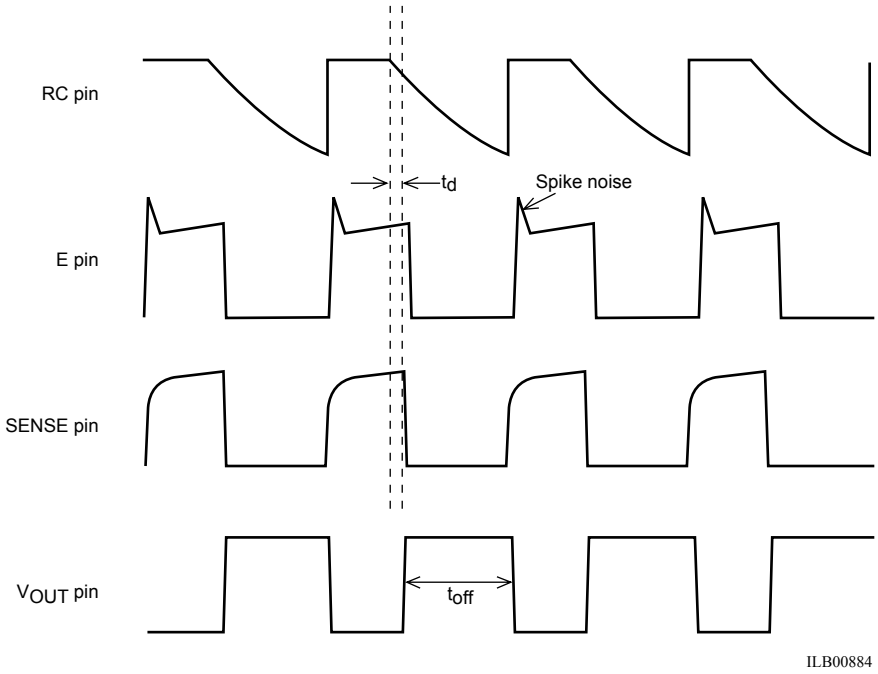


Figure 1 Switching Waveforms

t_{off}: Output off time. Determined by external capacitor and resistor Ct and Rt. (toff ≈ Ct × Rt)
t_d: Delay time between the point the set current is sensed at the SENSE pin and the point the output turns off.

Usage Notes

1. External diode
   Since this IC adopts a system based on lower side transistor switching drive, an external diode for the regenerative current that occurs during switching is required between V_{BB} and V_{OUT}. Use a Schottky barrier diode with a low feedthrough current.

2. Noise filters
   Since spike noise (see Figure 1) occurs when switching to the on state due to the external diode's feedthrough current, applications must remove noise from the SENSE pin with a noise filter (Cc, Rc) between the E pin and the SENSE pin.
   However, note that if the values of Cc and Rc are too large, the SENSE voltage rise will be slowed, and the current setting will be shifted towards a higher current level.

3. V_{REF} pin
   It is possible to change the output current continuously by continuously changing the V_{REF} pin voltage. However, this voltage cannot be set to 0V. The V_{REF} pin input impedance is 26kΩ (±30%) when V_{REF} is 5V. Since this pin is used to set the output current, applications must be designed so that noise does not appear on this pin's input.

4. GND pin
   Since this IC switches large currents, care must be taken to avoid ground loops when the IC is mounted in the application. The section of the PCB that handles large currents should be designed with a low-impedance pattern, and must be separated from the small signal sections of the circuit. In particular, the ground for the sense resistor Re must be as close as possible to the IC ground.

5. Operation in hold mode
   There are cases where a current somewhat larger than the current setting may flow in hold mode (light load mode). Since this IC adopts a lower side switching, lower side sense system, the emitter voltage falls and the sense voltage goes to 0 when the switching state goes to off. The circuit then always turns the output on after the toff period has elapsed. At this time, due to the light load, the existence of the time td, and the fact that the output goes on even if the output current is higher than the set current, the output current will be somewhat higher than the set current. Applications should set the current setting somewhat lower than required if this occurs.

6. Function for preventing the upper and lower outputs being on at the same time
   This IC incorporates a built-in circuit that prevents the through currents that occur when the phase is switched. The table lists the output on and off delay times when PHASE and EANBLE are switched.

		Sink side	Source side
When PHASE is switched	On delay time	10μs	9μs
	Off delay time	1.5μs	3μs
When ENABLE is on	On delay time	9μs	9μs
	Off delay time	1.5μs	6.5μs

7. 1-2 phase excitation and the double 1-2 phase excitation control sequence
   To reduce the vibration that occurs when the motor turns, this IC supports 1-2 phase excitation and double 1-2 phase excitation by using the output current setting digital input pins I_0 and I_1 without changing the V_{REF} pin voltage. Tables 1 and 2 list that control sequence, and Figure 2 and Figure 3 present the composite vector diagram for this sequence.2. Noise filters

Table 1 [1-2 phase excitation] 1/2 Step

ENABLE1 = ENABLE2 = 0

No	Phase A				Phase B			
	PH1	$I_1$1	$I_0$1	Current Value	PH2	$I_1$2	$I_0$2	Current Value
0	0	0	0	1	*	1	1	0
1	0	0	1	2/3	0	0	1	2/3
2	*	1	1	0	0	0	0	1
3	1	0	1	2/3	0	0	1	2/3
4	1	0	0	1	*	1	1	0
5	1	0	1	2/3	1	0	1	2/3
6	*	1	1	0	1	0	0	1
7	0	0	1	2/3	1	0	1	2/3

Table 2 [Double 1-2 phase excitation] about 1/4 Step

ENABLE1 = ENABLE2 = 0

No	Phase A				Phase B			
	PH1	$I_1$1	$I_0$1	Current Value	PH2	$I_1$2	$I_0$2	Current Value
0	0	0	0	1	*	1	1	0
1	0	0	0	1	0	1	0	1/3
2	0	0	1	2/3	0	0	1	2/3
3	0	1	0	1/3	0	0	0	1
4	*	1	1	0	0	0	0	1
5	1	1	0	1/3	0	0	0	1
6	1	0	1	2/3	0	0	1	2/3
7	1	0	0	1	0	1	0	1/3
8	1	0	0	1	*	1	1	0
9	1	0	0	1	1	1	0	1/3
10	1	0	1	2/3	1	0	1	2/3
11	1	1	0	1/3	1	0	0	1
12	*	1	1	0	1	0	0	1
13	0	1	0	1/3	1	0	0	1
14	0	0	1	2/3	1	0	1	2/3
15	0	0	0	1	1	1	0	1/3

Composite Vector Diagram

[1-2 phase excitation]

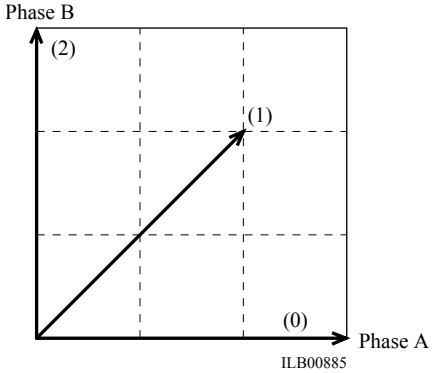


Figure 2 Composite Vector Diagram for the Sequence in Table 1 (1/4 cycle)

[Double 1-2 phase excitation]

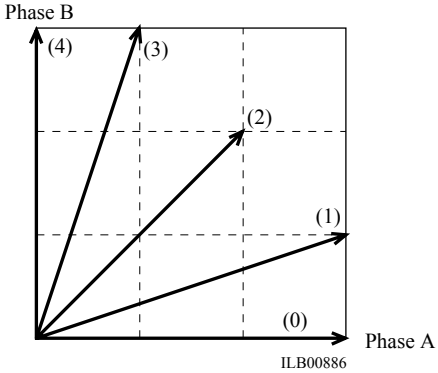
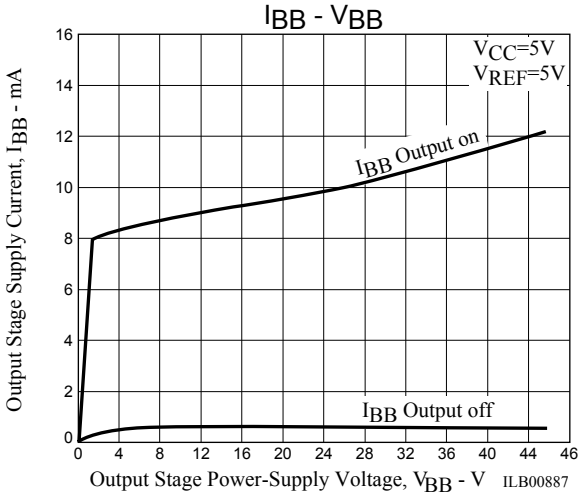
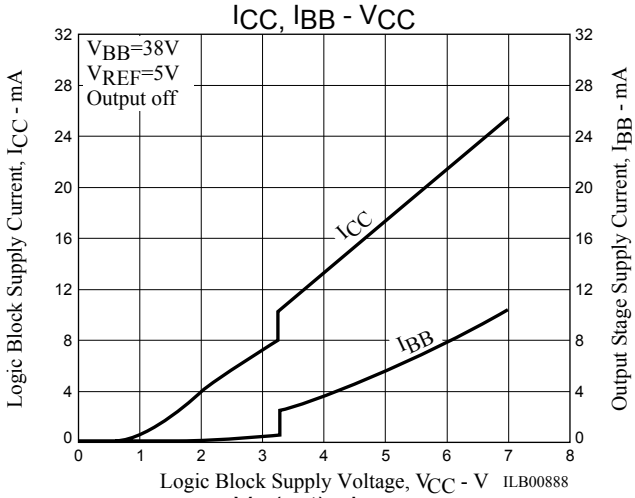
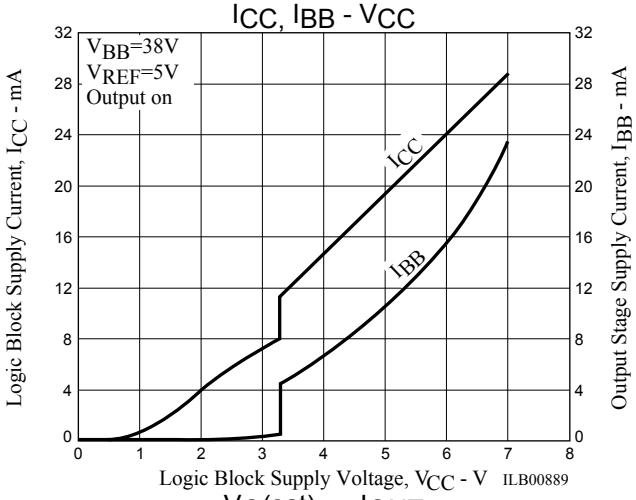
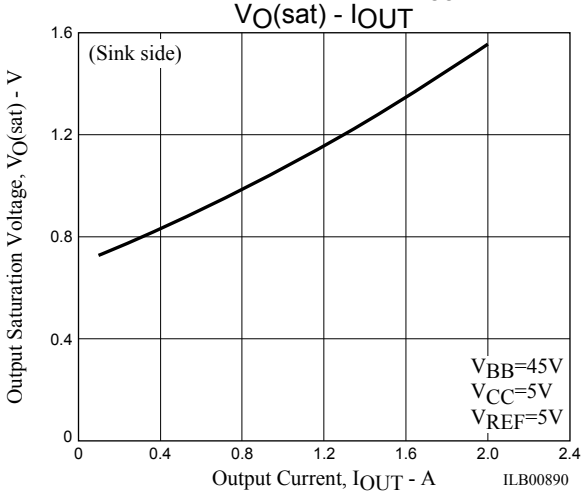


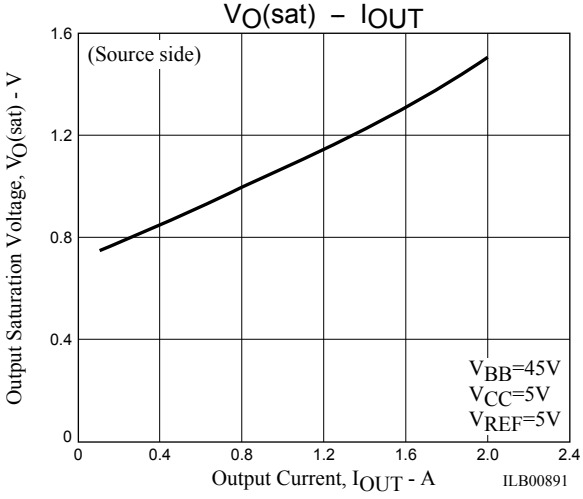
Figure 3 Composite Vector Diagram for the Sequence in Table 2 (1/4 cycle)


IBB - VBB
VCC=5V
VREF=5V
IBB Output on
IBB Output off
Output Stage Supply Current, IBB - mA
Output Stage Power-Supply Voltage, VBB - V
ILB00887


ICC, IBB - VCC
VBB=38V
VREF=5V
Output off
ICC
IBB
Logic Block Supply Current, ICC - mA
Output Stage Supply Current, IBB - mA
Logic Block Supply Voltage, VCC - V
ILB00888


ICC, IBB - VCC
VBB=38V
VREF=5V
Output on
ICC
IBB
Logic Block Supply Current, ICC - mA
Output Stage Supply Current, IBB - mA
Logic Block Supply Voltage, VCC - V
ILB00889


VO(sat) - IOUT
(Sink side)
VBB=45V
VCC=5V
VREF=5V
Output Saturation Voltage, VO(sat) - V
Output Current, IOUT - A
ILB00890


VO(sat) – IOUT
(Source side)
VBB=45V
VCC=5V
VREF=5V
Output Saturation Voltage, VO(sat) - V
Output Current, IOUT - A
ILB00891

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