PIC32MM0064GPL036 Family Silicon Errata and Data Sheet Clarification

The PIC32MM0064GPL036 family devices that you have received conform functionally to the current Device Data Sheet (DS60001324**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MM0064GPL036 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B0**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC32MM0064GPL036 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)
		B0
PIC32MM0016GPL020	06B04053	0004
PIC32MM0032GPL020	06B0C053	
PIC32MM0064GPL020	06B14053	
PIC32MM0016GPL028	06B02053	
PIC32MM0032GPL028	06B0A053	
PIC32MM0064GPL028	06B12053	
PIC32MM0016GPL036	06B06053	
PIC32MM0032GPL036	06B0B053	
PIC32MM0064GPL036	06B16053	

Note 1: The Device IDs and Revision ID (DEVID and DEVREV) are shown in hexadecimal format.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				B0
ADC	12-Bit Mode Conversion	1.	ADC has missing codes.	X
ADC	Format Options	2.	ADC format option is incorrect.	X
Reset	$\overline{\text{MCLR}}$ Pin	3.	$\overline{\text{MCLR}}$ Reset does not work in Retention Sleep mode.	X
UART	Receive Buffer Overflow Detection	4.	Overflow disable feature is not functional.	X
Primary XT and HS Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	5.	OST may indicate oscillator is ready for use and set the POSCRDY bit (CLKSTAT<2>) too early.	X
Reset	Current Consumption	6.	Current consumption in Master Clear Reset is high.	X
Reset	Configuration Mismatch Reset (CMR)	7.	An erroneous Configuration Mismatch Reset (CMR) event may occur after a POR, BOR or external device programming (ICSP™ or JTAG).	X
Timer1	External Clock Mode	8.	External Clock Mode: Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.	X
Timer1	External Clock Mode	9.	External Clock Mode: The first increment value is not visible when using External Clock mode and a 1:1 prescaler.	X
Power	Retention Sleep	10.	Retention Sleep: When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X
Power	BOR	11.	BOR: The main BOR may not function.	X
Programming	JTAG TDO Pin	12.	The JTAG TDO (RB10) pin toggles during programming when using the PGECx/PGEDx pairs.	X
I/O	Schmitt Trigger Inputs	13.	Schmitt trigger inputs may have glitches with slow signal rise/fall times.	X
SPI	SRMT Bit	14.	In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B0**).

1. Module: ADC

The 1023, 2046, 2047, 3070 and 3071 codes may be missing in 12-bit mode.

Work around

Use 10-bit mode if all codes are desired in the application.

Affected Silicon Revisions

B0							
X							

2. Module: ADC

The ADC result of the 32-bit signed format option (FORM<2:0> bits = b101) is the same as the result of the 16-bit signed format option (FORM<2:0> = b001).

Work around

In the software, expand the Data Output Format bits to convert the output format from 16-bit signed integer to 32-bit signed integer.

Affected Silicon Revisions

B0							
X							

3. Module: Reset

$\overline{\text{MCLR}}$ is not a source of wake-up from Retention Sleep mode. Reprogramming the device may not work when the device is in Retention Sleep.

Work around

Use other wake-up sources (such as an external interrupt or Change Notification interrupt) or implement other means in the application to prevent entering into Retention Sleep mode during programming.

Affected Silicon Revisions

B0							
X							

4. Module: UART

The receive buffer overflow disable feature, controlled by the OVFDIS bit, is not functional.

Work around

None.

Affected Silicon Revisions

B0							
X							

5. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use and set the POSCRDY bit (CLKSTAT<2>) too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize POSC.
3. Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma  config FNOSC = FRCDIV           // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma  config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
void main()
{
    // configure REFO to request POSC
    REFO1CONbits.ROSEL = 2;              // POSC = 2
    REFO1CONbits.OE = 0;                 // disable output
    REFO1CONbits.ON = 1;                 // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {                                    // delay for 9 ms
        unsigned int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
    }

    // unlock OSCCON
    SYSKEY = 0;
    SYSKEY = 0xAA996655;
    SYSKEY = 0x556699AA;
    // switch to POSC = 2
    OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
    OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
    while(OSCCONbits.OSWEN == 1);        // wait for switch
```

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
    // Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
    #pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    // unlock OSCCON
    SYSKEY = 0;
    SYSKEY = 0xAA996655;
    SYSKEY = 0x556699AA;
    // switch to FRC = 0 before entering to sleep
    OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
    OSCCONSET = (0<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
    while(OSCCONbits.OSWEN == 1);            // wait for switch

    // enter sleep mode
    asm     volatile("wait");

    // configure REFO to request POSC
    REFO1CONbits.ROSEL = 2;                  // POSC = 2
    REFO1CONbits.OE = 0;                     // disable output
    REFO1CONbits.ON = 1;                     // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {                                        // delay for 9 ms
        unsigned int start = __builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT);
while((__builtin_mfc0(_CP0_COUNT, _CP0_COUNT_SELECT)) - start < (unsigned int)(0.009*8000000/2));
    }

    // switch to POSC = 2
    OSCCONCLR = _OSCCON_NOSC_MASK | _OSCCON_CLKLOCK_MASK | _OSCCON_OSWEN_MASK;
    OSCCONSET = (2<<_OSCCON_NOSC_POSITION) | _OSCCON_OSWEN_MASK;
    while(OSCCONbits.OSWEN == 1);            // wait for switch
```

Affected Silicon Revisions

B0							
X							

6. Module: Reset

When Master Clear ($\overline{MCLR}$) is asserted, the current consumption is higher than the Reset IPD specification.

Work around

Do not use $\overline{MCLR}$ to hold the device in Reset to save power.

Affected Silicon Revisions

B0							
X							

7. Module: Reset

An erroneous Configuration Mismatch Reset (CMR) event may occur after a POR, BOR or external device programming (ICSP™ or JTAG). This event will cause a device POR Reset and set the CMR bit in the RCON register.

Work around

Clear the CMR bit in the RCON register.

Affected Silicon Revisions

B0							
X							

8. Module: Timer1

Timer1 does not overflow in External Clock mode when PR1 = 1 and the prescaler is 1:1.

Work around

Use a PR1 value greater than one.

Affected Silicon Revisions

B0							
X							

9. Module: Timer1

The first increment value is not visible when using External Clock mode and a 1:1 prescaler.

Work around

None.

Affected Silicon Revisions

B0							
X							

10. Module: Power

When the device wakes up from Retention Sleep mode, a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set for this Reset.

Work around

To provide a consistent behavior when the device wakes up from the Retention Sleep mode, the software Reset sequence should be performed following the `WAIT` instruction (refer to Example 3). In this case, a Reset will always be generated when the device wakes up from Retention Sleep.

EXAMPLE 3: SOFTWARE RESET CODE EXAMPLE

```
unsigned int dummy;
SYSKEY = 0x00000000;          // write invalid key to force lock
SYSKEY = 0xAA996655;          // write key1 to SYSKEY
SYSKEY = 0x556699AA;          // write key2 to SYSKEY
RSWRSTSET = 1;                // set SWRST bit to arm reset
dummy = RSWRST;               // read RSWRST register to trigger reset
while(1);                     // prevent any unwanted code execution until reset occurs
```

Affected Silicon Revisions

B0							
X							

11. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values.

Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

B0							
X							

12. Module: Programming

The JTAG TDO (RB10) pin toggles during programming when using the ICSP™ pairs.

Work around

For 20-pin devices: Do not connect external circuitry to the TDO pin (RB12) that cannot tolerate toggling when programming using the PGEC1/PGED1, PGEC2/PGED2 or PGEC3/PGED3 pins.

For 28-pin, 36-pin and 40-pin devices: Do not connect external circuitry to the TDO pin (RB10) that cannot tolerate toggling when programming using the PGEC1/PGED1 or PGEC3/PGED3 pins.

Affected Silicon Revisions

B0							
X							

13. Module: I/O

If the input signal rise or fall time is more than 500 nS, the I/O Schmitt Trigger output may have glitches.

Work around

The rise/fall time of the input signal must be less than 500 nS.

Affected Silicon Revisions

B0							
X							

14. Module: SPI

In SPI Slave mode, the SRMT bit may be set if the FIFO or Shift register is not empty.

Work around

The following work arounds can be implemented in the application to detect when the FIFO and Shift register are empty:

1. Check the SPITBF bit before checking the SRMT bit. If the SPITBF flag is cleared and the SRMT flag is set, then all data was transmitted. Example 4 demonstrates the SPITBF and SRMT bits polling.
2. Read the SRMT bit twice, back-to-back. If the SRMT bit is set two reads in a row, then the FIFO and Shift register are empty. Example 5 demonstrates the SRMT bit polling using double read.

EXAMPLE 4: EMPTY STATUS DETECTION USING SPITBF AND SRMT BITS POLLING

```
// Both flags must indicate empty status.
while(SPI1STATLbits.SPITBF);
while(!SPI1STATLbits.SRMT);
```

EXAMPLE 5: EMPTY STATUS DETECTION USING SRMT BIT POLLING WITH BACK-TO-BACK READS

```
// If SRMT bit is set two reads in a row
   then it set correctly.
asm  volatile("\n\
la   $t0, SPI1STAT;\
loop:;\
lw   $t1, 0($t0);\
lw   $t2, 0($t0);\
and  $t1, $t1, $t2;\
andi $t1, $t2, 0x80;\
beqz $t1, loop;");
```

Affected Silicon Revisions

B0							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001324**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (4/2016)

Initial release of this document; issued for silicon revision B0.

Rev B Document (6/2016)

Corrected the codes in silicon issue 2 (ADC).

Added silicon issue 5 (Primary XT and HS Oscillator (POSC)).

Rev C Document (4/2017)

Updated Table 2.

Added silicon issues 6 (Reset), 7 (Reset), 8 (Timer1), 9 (Timer1), 10 (Power), 11 (Power), 12 (Programming), 13 (I/O) and 14 (SPI).

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