International
IOR Rectifier

Automotive Grade

AUIR3330S

PROTECTED HIGH FREQUENCY HIGH SIDE SWITCH
FOR AUTOMOTIVE DC MOTOR DRIVE

Features

- Up to 30Khz PWM switching capability
- Charge pump for DC operation
- Active di/dt control to reduce EMI
- Load current feedback
- Short-circuit protection
- Programmable over current shutdown
- Over temperature shutdown
- Diagnostic feedback
- Under voltage shutdown
- Gnd, IN and bootstrap pin loss protection
- E.S.D protection
- Low power mode
- Lead-free, RoHS compliant

Product Summary

Rds(on)@25°C	3.5mΩ max.
Max current	65A
Operating voltage	6 -18V

Application

- Fan engine cooling
- Air conditioning blower
- Pumps (oil, fuel, water…)
- Compressor

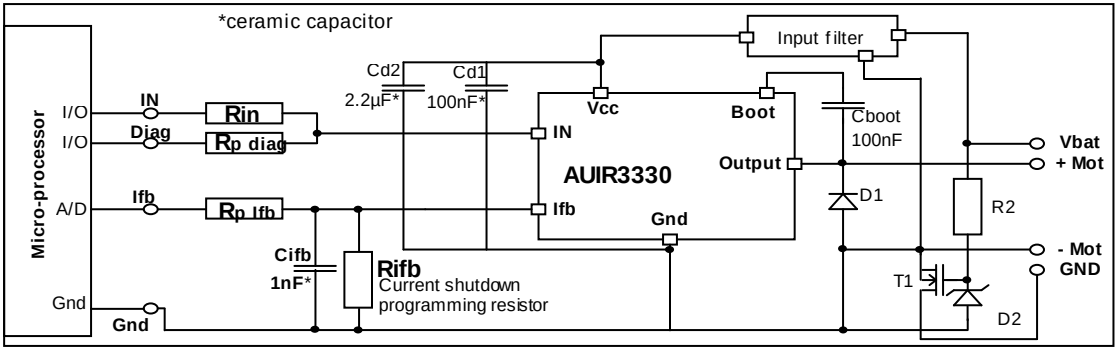
Packages

AUIR3330S
D2Pak - 7 leads

Description

The AUIR3330s is a 7 terminals high side switch for variable speed DC motor. It features simplify the design of the DC motor drive with a microcontroller. The Mosfet switches the power load proportionally to the input signal duty cycle at the same frequency and provides a current feedback on the Ifbk pin. The over-current shutdown is programmable from 5A to 50A. Over-current, over-temperature latch OFF the power switch, providing a digital diagnostic status on the input pin. In sleep mode, the device consumes typically less then 1uA. Further integrated protections such as ESD and GND disconnect protection guarantee safe operation in harsh conditions of the automotive environment.

Typical connection with reverse battery protection



Qualification Information†

Qualification Level		Automotive (per AEC-Q100††) Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.
Moisture Sensitivity Level		MSL1 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M3 (+/-350V) (per AEC-Q100-003)
	Human Body Model	Class H4 (+/-4000V) (per AEC-Q100-002)
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)
IC Latch-Up Test		Class II Level A (per AEC-Q100-004)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/
†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. (Tj= -40°C..150°C, Vcc=6..18V unless otherwise specified).

Symbol	Parameter	Min.	Max.	Units
Vout	Maximum drain to source voltage	GND-5V	Vcc+0.3	V
Vin	Maximum input voltage	-0.3	5.5	V
Vcc max.	Maximum Vcc voltage	—	36	V
Vcc cont	Maximum continuous Vcc voltage	—	28	V
Iin max.	Maximum input current	-0.3	10	mA
Ifb max	Maximum Ifb current	-50	10	mA
Pd	Maximum power dissipation Rth=60°C/W Tambient=25°C, Tj=150°C Rth=40°C/W D²Pack 6cm² footprint	—	2.5	W
Tj max.	Max. storage & operating temperature junction temperature	-40	150	°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
Rth1	Thermal resistance junction to ambient D²Pak Std footprint	60	—	°C/W
Rth2	Thermal resistance junction to ambient D²pak 6cm² footprint	40	—	
Rth3	Thermal resistance junction to case D²pak	0.65	—	

Recommended Operating Conditions

These values are given for a quick design.

Symbol	Parameter	Min.	Max.	Units
Vcc op.	Operating voltage range	6	18	V
Iout	DC output current Tj=145°C, Tamb=85°C, Rth=5°C/W	—	45	A
Cboot	Bootstrap capacitor	100	220	nF
Cd1	Decoupling ceramic capacitor	100	—	nF
Cd2	Decoupling ceramic capacitor	2.2	—	µF
R In	Recommended resistor in series with In pin	1	5	kΩ
Rp diag	Recommended resistor in series with In pin to read the diagnostic	10	50	kΩ
Cifb	Recommended Ifb filter capacitor	1	2.2	nF
Rlfb	Recommended resistor to program over current shutdown	0.6	5	kΩ
Rp Ifb	Recommended resistor in series with Rlfb pin to read the current feedback	10	25	kΩ
F max.	Maximum recommended input frequency, duty cycle=10% to 90%	—	30	kHz

Static Electrical Characteristics

-40°C < Tj < 150°C, 6V < Vcc < 18V, (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Rds on	ON state resistance Tj=25°C	—	3	3.5	mΩ	Iout=30A
	ON state resistance Tj=150°C[1]	—	5.5	6.2		Iout=30A
Rds on Lv	ON state resistance low voltage Tj=25°C	—	3	3.5	mΩ	Iout=15A Vcc=6V
Vf Mos	Forward voltage of the Mosfet body diode	0.6	—	1.1	V	Iout = -50A
Vbrk out	Breakdown voltage between Vcc and Vout (MOSFET body diode)	39	40	—	V	
I Vcc Slp	Supply current in sleep mode (IC + MOSFET leakage)	—	1	2	µA	Vin=0V Vcc = 14V Tj = 25°C
I bias Boot	Bootstrap regulator biasing current (flows through the output)	—	5.5	14	mA	Vout = 0V
I Vcc Wke	Vcc current when the device is woken up (IC + Ibias Boot)	—	14	20	mA	I_boot = 0A Vout = 0V
V In Wke	Input threshold voltage to wake up the device	0.35	0.75	1	V	
V In Off	In voltage threshold to turn off	1.9	2.2	—	V	
V In On	In voltage threshold to turn on	—	2.8	3.2	V	
V In Hyst	Input threshold hysteresis	0.4	—	0.7	V	
C In	Input pin capacitor	-	10	-	pF	
I In on	On state input current	10	20	30	µA	Vin = 5V
I Bt Chrge	Bootstrap current charge	0.4	—	1.5	A	Vout = 0V Cboot =500nF
V Bt Chrge	Bootstrap voltage	4.9	5.5	6.3	V	Cboot =500nF

Guaranteed by design.

Switching Electrical Characteristics

-40°C < Tj < 150°C, 6V < Vcc < 18V, Rin = 5kΩ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Td Vout on	Turn-on output voltage delay time	0.7	1	1.4	µs	betw een 50% of IN and 30% of Vout, Iout = 14A
Tr Vout	Ouput voltage rise time	500	800	1300	ns	Betw een 15% and 85%; Vcc = 14v, Iout=14A
Tr Iout	Ouput current rise time	0.7	1.2	1.85	µs	Betw een 5A and 40A; Vcc = 14v, Iout=45A
dv/dt on	Turn on dv/dt	10	20	28	V/µs	Betw een 25% and 70%; Vcc = 14v
di/dt on	Turn on di/dt	21	40	51	A/µs	Betw een Iout 15A and 35A; Vcc = 14v
Td Vout off	Turn-off delay time	0.9	1.2	1.7	µs	betw een 50% of IN and 90% of Vout, Iout = 14A
Tf Vout	Output voltage fall time	250	430	650	ns	Betw een 90% and 10%; Vcc = 14v, Iout=14A
Tf Iout	Output current fall time	0.55	1	1.45	µs	Betw een 40A and 5A; Vcc = 14v, Iout=45A
dv/dt off	Turn off dv/dt	28	50	67	V/µs	Betw een 30% and 70%; Vcc = 14v
di/dt off	Turn off di/dt	30	40	51	A/µs	Betw een Iout 35A and 15A; Vcc = 14v
T Trfct Ld	Input output transfer function for low duty cycle	8.5	10	11.5	µs	Iout = 1A; In pulse time =10µS
T Trfct Hd	Input output transfer function for high duty cycle	38.5	39.5	40.5	µs	Iout = 1A; In pulse time =40µS
T Off Min	Minimum off time to recharge the bootstrap capacitor	—	—	2	µs	Cboot = 100nF

Protection Characteristics

-40°C < Tj < 150°C, 6V < Vcc < 18V (unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Vth Ifb	IFB over current threshold voltage	3.65	4	4.35	V	
Isd fix	Maximum internal over current shutdown	55	70	90	A	
Isd prog 2	Programmable current shutdown	11	17	24	A	Rifb = 1.5kΩ
Isd prog 1	Programmable current shutdown	30	40	50	A	Rifb = 640Ω
Tsd	Over temperature threshold[2]	150	165	175	°C	
Vth Vds OVP	Vds threshold to activate the over power protection	—	0.75	—	V	Tj=25°C
Td Vds OVP	Vds delay to turn off after OVP detection	6	10	15	µs	
UV On	Under voltage threshold to turn on	—	5.3	6.3	V	
UV Off	Under voltage threshold to turn off	—	4.3	5.3	V	
UV Hyst	Under voltage hysteresis	0.5	—	1.25	V	
T slp	Sleep mode time and fault reset	20	30	50	ms	
T rst	Time to reset the latched fault	—	50	—	µs	Tj=25°C
T wke min	Minimum pulse width to wake up	2	—	—	µs	
Tpwr_on_rst	Power on reset time	5	8	15	µs	
F Dg OT	Over temperature diagnostic frequency	—	260	—	Hz	
F Dg OC	Over current diagnostic frequency	35	70	95	Hz	
V Dg Dft	DG voltage when fault	—	—	400	mV	Vin = 5V Rin = 5kΩ

Current Sense Characteristics

-40°C < Tj < 150°C, 6V < Vcc < 18V (unless otherwise specified), Rifbk=1kΩ

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I offset	Load current diagnostic offset	-2.7	0.62	4	A	Range 5A to 40A
Ratio	(Iload + I offset) / Ifb	5400	6400	7200	—	Range 5A to 40A
Ratio Tc	Iload/Ifbk variation over temperature	-3.5	-	1.5	%	Tj=-40°C to 150°C

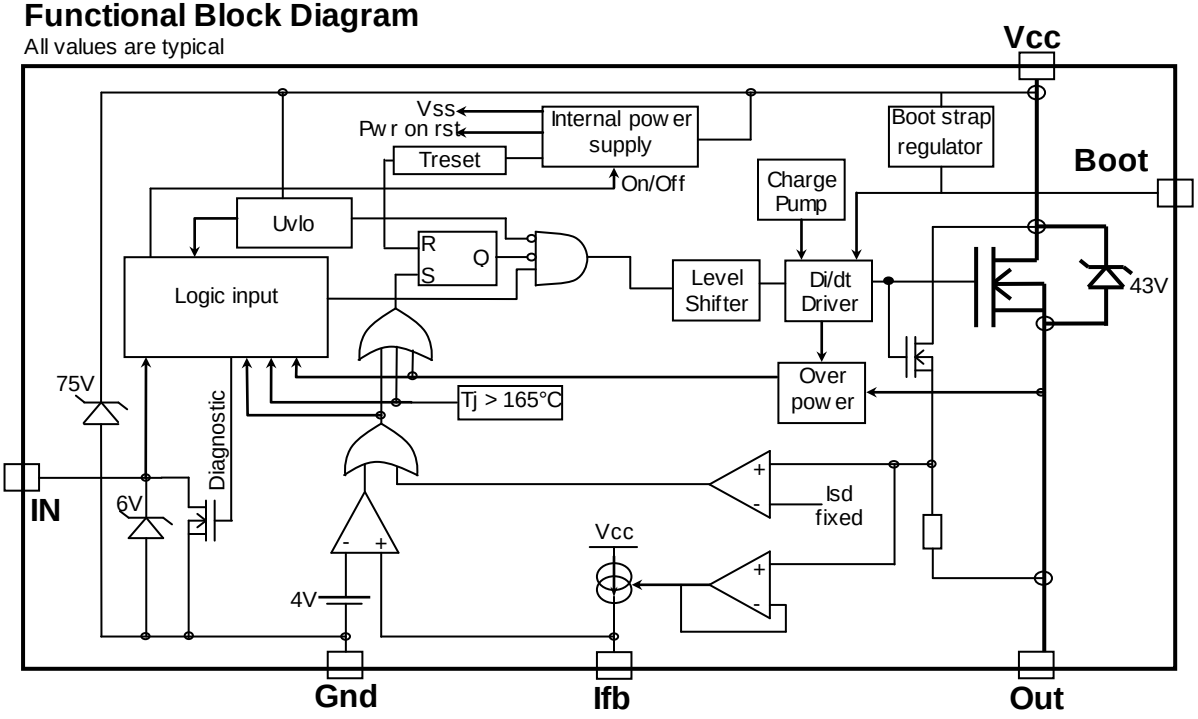
[2] Guaranteed by design.

Leads Assignment

PART NUMBER	AUIR3330S
1 : Ifb 2 : In 3 : Gnd 4 : Vcc (Tab) 5 : Boot 6 : Out 7 : Out	 D2Pak 7 leads

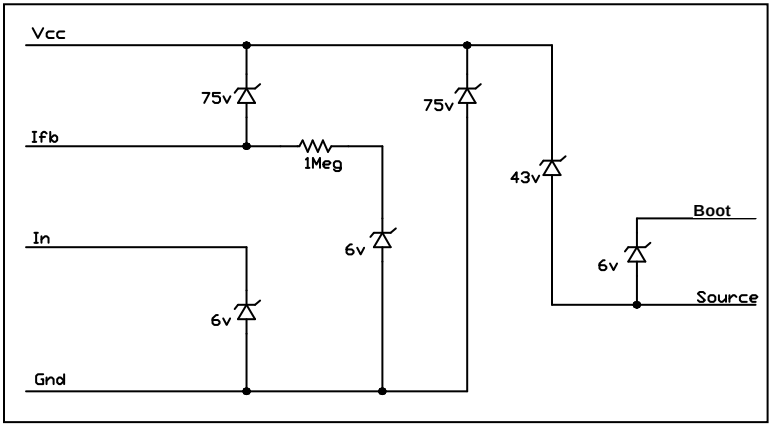
Functional Block Diagram

All values are typical



Internal diode schematic

All values are typical



Design: basic schematic with microprocessor

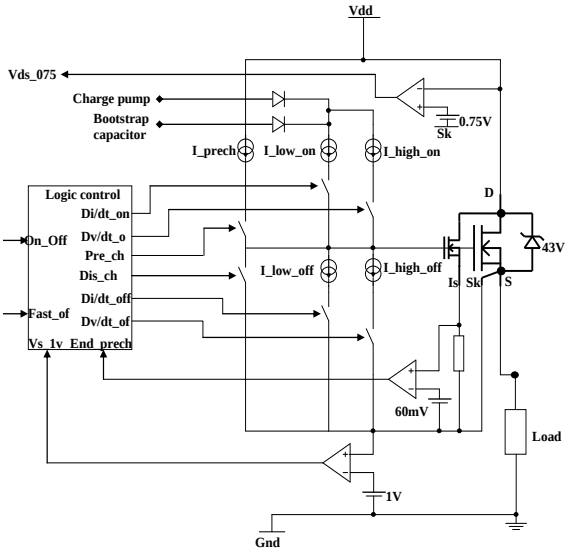
The basic circuit is giving all the functionality to drive a 50A DC motor. Rlfb set both the current shutdown and the current feedback reading scale. The In signal provides the Pwm frequency and duty cycle order to the AUIR3330S. D1 is the free wheeling diode during PWM operation. As the equivalent circuit between Vbat and – Mot is 2 diode in series (the body diode of the AUIR3330S and D1), the system requires T1, D2, R1 and R2 to sustain the reverse battery. (Cf: Typical connection with reverse battery protection).

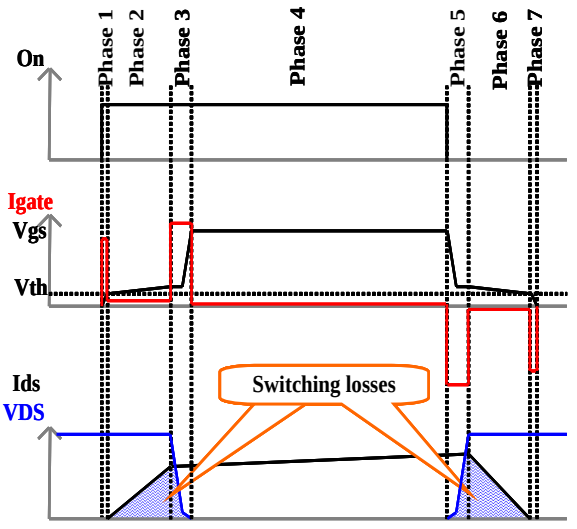
DC to 30 kHz operation

The AUIR3330S is able to operate in DC and high speed switching operation. To be able to switch at 30 kHz, a bootstrap capacitor is used externally. The device integrates the power supply of the bootstrap capacitor. In DC operation, when the capacitor is discharged, the charge pump maintains the device ON.

Active di/dt control to reduce EMI and switching losses

The AUIR3330S includes a special gate drive, managing the Mosfet di/dt controlled internally, by managing the gate voltage dynamically. This di/dt trade-off is set internally to an optimum value, between power dissipation versus noise. This feature brings to the designer less EMI versus switching losses. The system has three phases during the turn on sequence and three phases during the turn off sequence. First the driver injects a high current in the gate until the gate voltage reaches the Vth. Then it injects a low current to control the di/dt value until the gate voltage reaches the miller plate. And after it injects a high current to fully turn on quickly the MOSFET to reduce the dv time (reducing the switching losses). The turn off sequence is the same than the turn on but in the opposite direction: First reduce the dv time after control the di/dt and then discharge totally the gate.





Sense Load current feedback and programmable current shutdown

The Ifb pin allows an analog measurement of the load current and with an external resistor allows to program the over current shutdown level from 10A to 50A. The voltage threshold level of the Ifb pin is internally set to 4v (See the formulas below). It is also possible to dynamically adjust the current shutdown protection versus time by adding some external components. This protection is latched and turns off the output MOSFET without di/dt sequence to reduce the device and the application stress. The operating mode is recovered after resetting by the sleep mode.

$$Rifb = \frac{Vifb\_gnd\min}{Imax\_appli + Ioffset\min} \times Ratio\min$$

$$Ishd\max = MAX\left[Ishd\max@-40°C; Ishd\max@25°; Ishtd\max@150°C\right]$$

$$Ishd\max@T°C = \left[\frac{Vifb\_gnd\max}{Rifb(calculated)} \times Ratio\max@T°C\right] + Ioffset\max@T°C$$

$$Vifb\min@T°C = \frac{Iload - Ioffset\max@T°C}{Ratio\max@T°C} \times Rifb$$

$$Vifb\max@T°C = \frac{Iload - Ioffset\min@T°C}{Ratio\min@T°C} \times Rifb$$

Where:

Imax appli is the maximum application current
Ishtd max is the maximum output shutdown current

Internal over current shutdown

The maximum current shutdown threshold value is internally fixed to 65A typ. This protection is latched and turns off the output MOSFET without di/dt sequence to reduce the device and the application stress. The operating mode is recovered after resetting by the sleep mode.

Under voltage lock-out

The AUIR3330S remains operational from UV off threshold. Under this continuous voltage, the device will be locked until the voltage recovers the operating range, according to an internal hysteresis fixed to 0,5V min. The maximum rating voltage is given by the Trench VDMOS technology where the avalanche voltage is up to 43V typically.

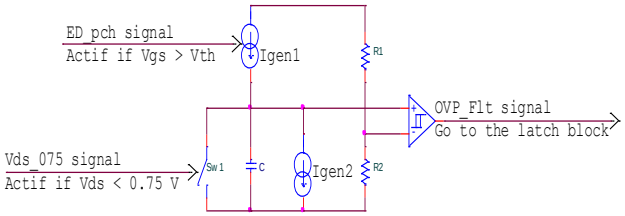
Sleep mode and reset fault:

The sleep mode is enabled if the IN pin stay low (Vin < V In Slp) more than T Slp time. The consumption in sleep mode is Icc off. The AUIR3330S wakes up at first rise edge on the IN pin (Vin > V In Slp). This mode allows resetting all the latched faults after Trst time (Cf. Figure 1: Wake sequence, sleep mode and reset latched fault protocol). This filter time allows memorizing and maintaining the fault latched even if the power supply is removed (ISO pulses latch protection).

Over-power protection

The AUIR3330S have an internal over-power protection. This feature allows protecting the silicon device and the application against several critical issues:

- The bootstrap capacitor missing.
- Abnormal leakage on the bootstrap capacitor.
- Abnormal leakage on the power MOSFET gate.
- Very low impedance output short circuit.



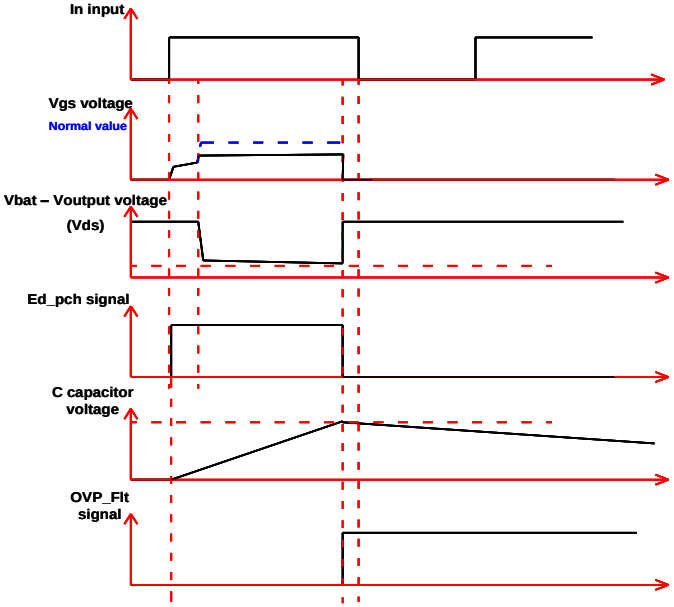
Time to charge the capacitor and latch a fault (Igen1 + C) = 9µs
Time to discharge the capacitor (Igen2 + C) = 11ms

- The time constant Ign1 + C represent the thermal silicon time constant
- The time constant Ign2 + C represent the thermal package time constant (T(ign2 + C) < T Slp)
- Igen1 is on if the gate voltage (of the output MOSFET) is higher than its Vth
- Ign2 is always switching on.
- Sw 1 is close if the Vbat – out voltage (Vds) is lower than 0.75V

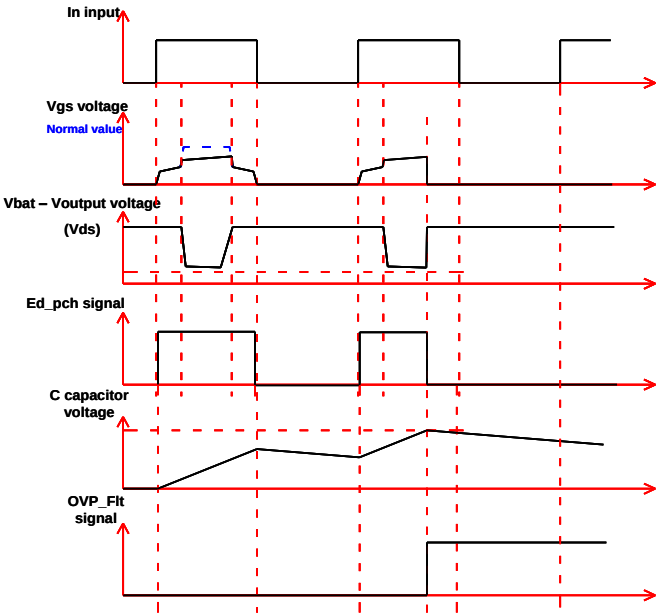
When the Output MOSFET gate voltage reaches its output MOSFET Vth value, the current generator Igen1 start to charge the capacitor C. Then three scenarios are possible:

1. The device turn on properly (Vds < 0.75v) and the capacitor C is discharged by the switch sw 1. The device is ready for the next pulse. It is the normal case.

2. The device can not turn on properly (Vds stay > 0.75v no capacitor reset) and the on time duration (duty cycle) is enough long to charge completely the capacitor C. The comparator detects the fault, stop the device and latch it. This fault could be reset by a sleep mode



3. The device can not turn on properly (Vds stay > 0.75v no capacitor reset) but the ON time duration (duty cycle) is not enough long to charge completely the capacitor C. So the fault is not detected by the comparator and it is not latched. But the picture of energy value dissipated by the MOSFET during the almost turn on value is stored in the capacitor C. And at the next pulse the current generator Igen1 resume to charge the capacitor until it reach the comparator value and latch the fault (this sequence could be on several pulse). It could be reset by a sleep mode.



Wake up sequence:

The AUIR3330S has an internal power on reset. After waking it up by the IN signal, the device waits for Tpwron_rst before activating the output power mosfet. This time is required to charge properly the bootstrap capacitor and to stabilize the internal power supply (Cf. Figure 1: Wake sequence, sleep mode and reset latched fault protocol).

In pin and digital diagnostic

The IN has two functions. In normal working condition, the output follows the IN pin digital level. In latched fault condition (over current and over temperature shutdown), the IN pin provides a digital feedback to the µ-processor. This digital diagnostic gives a different frequency signal according to the fault type.

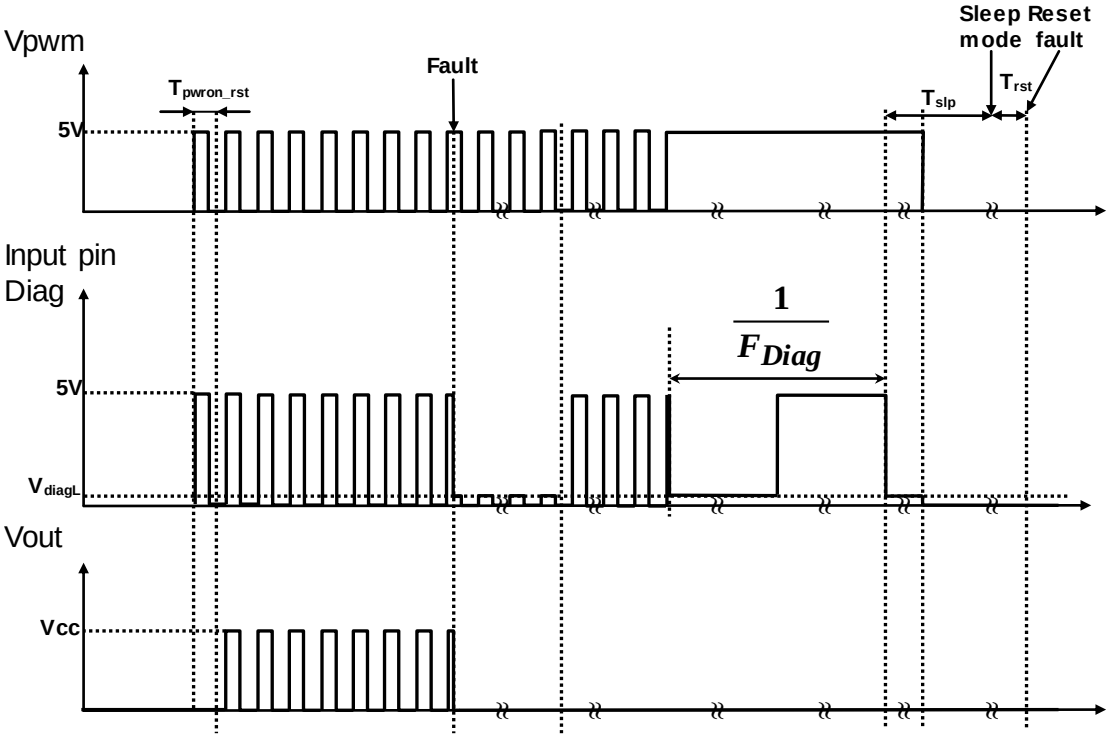
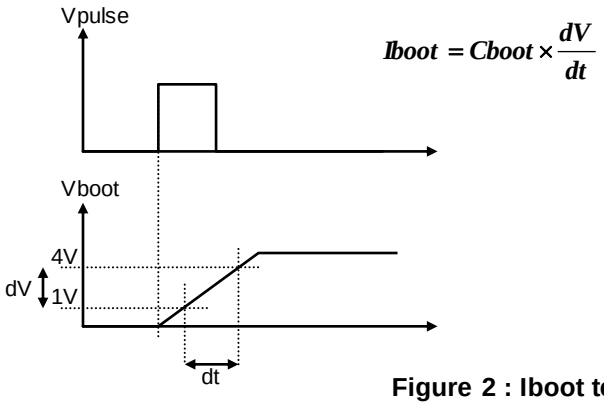


Figure 1: Wake sequence, sleep mode and reset latched fault protocol

Bootstrap current measurement:



$$Iboot = Cboot \times \frac{dV}{dt}$$

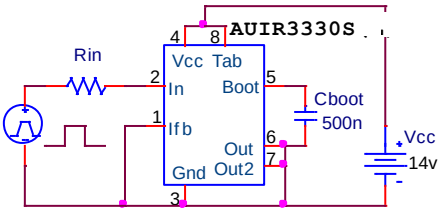


Figure 2 : Iboot test circuit

Switching time definition:

As the opposite schematic shows, the dv/dt on & off and the Td Vout on & off switching time are measured at zero current value and with a simulated continuous conduction condition to avoid the di/dt impact (see also the chronogram above).
Due the inductive load, the drain current level impacts directly the delay to switch on the output voltage. So the output voltage duty cycle value changes with the current level. The output current duty cycle is higher than the output voltage duty cycle. The di/dt on limit value allows calculating the complete delay (here named Tcdon and off) to switch on the output voltage.

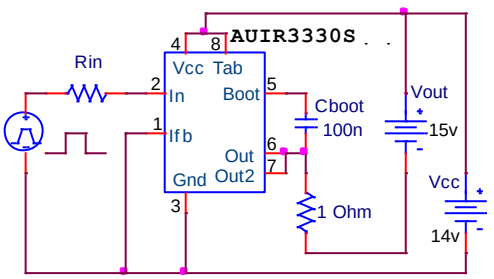


Figure 3: Switching time test circuit

$$Tcdon_{\max} = Td\_Vout\_on_{\max} + \frac{Id}{didt\_on_{\min}}$$

$$Tcdon_{\min} = Td\_Vout\_on_{\min} + \frac{Id}{didt\_on_{\max}}$$

$$Tcdoff_{\min} = Td\_Vout\_off_{\min}$$

$$Tcdoff_{\max} = Td\_Vout\_off_{\max}$$

$$Ton_{\min} = Tin\_on - Tdcon_{\max} + Tcdoff_{\min}$$

$$Ton_{\max} = Tin\_on - Tdcon_{\min} + Tcdoff_{\max}$$

All switching time values (except the Td Vout on & off parameters) could change with the application schematic (output snubber filter) and with the PCB layout. Due to the internal pad, the input pin of the device has a parasitic capacitor Cin. This capacitor and the Rin (the recommended input resistor) create low pass filter and add an additional delay in the Tdcon value.

The minimum off time is the time to charge the bootstrap capacitor (recover the value before turn on the MOSFET) during the high duty cycle operation. In the high duty cycle value condition, due to the di/dt driver, the internal gate continues to move whereas the output voltage doesn't go down under 6v (from vbat). So the device still need energy from the bootstrap capacitor but it can not charge it. When the bootstrap capacitor is discharged the circuit goes in linear mode and it is stopped by the over power protection. To avoid this situation, the micro-processor must turn fully on the device after the minimum off time is reached as it is describe in the Figure 5: High duty cycle operation recommendation. The minimum off time is the minimum time to charge properly the bootstrap capacitor.

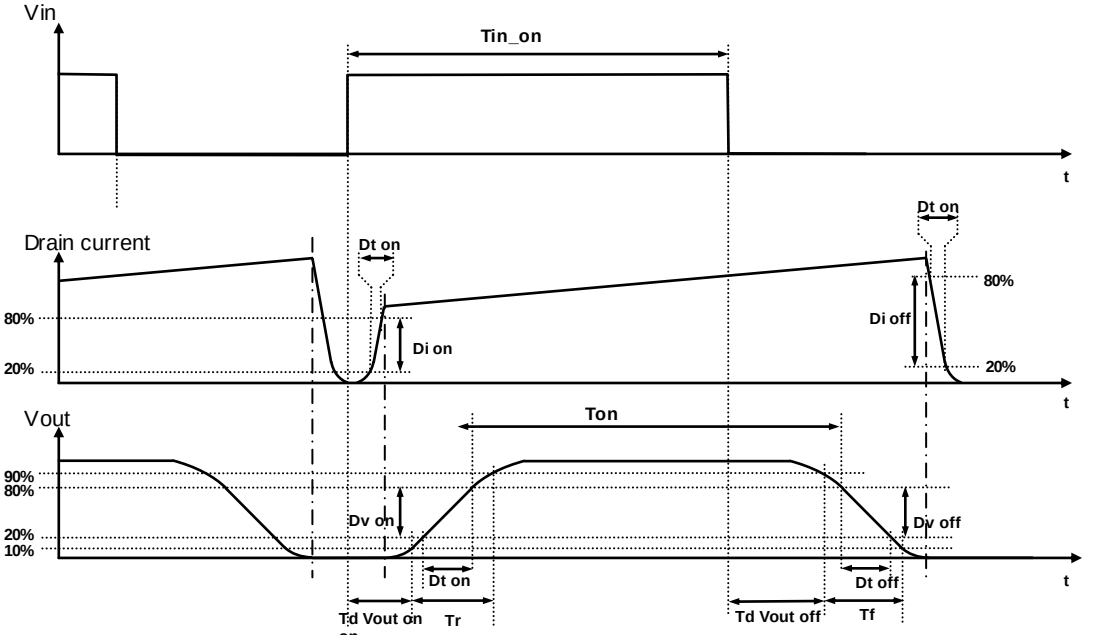


Figure 4 : Switching time chronogram

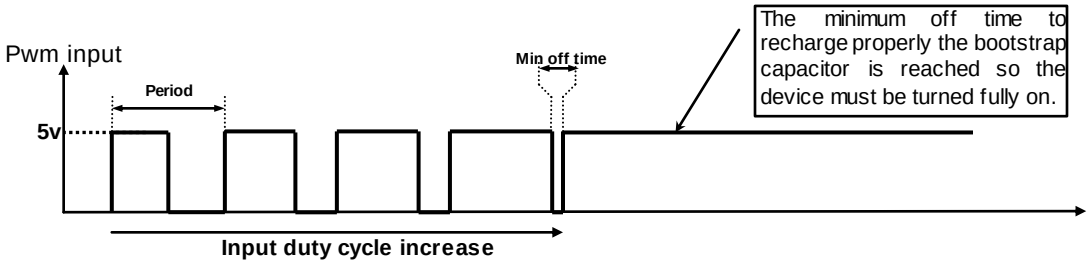
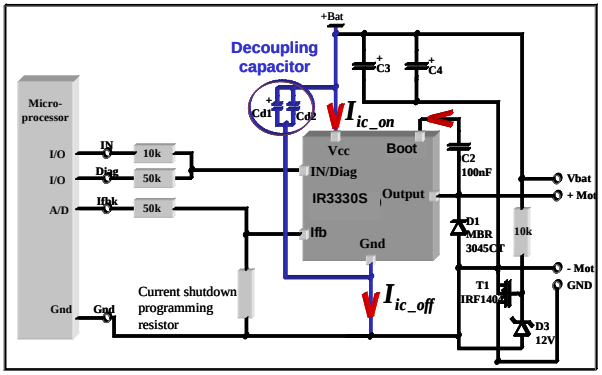


Figure 5: High duty cycle operation recommendation

Notes:

Decoupling capacitors:

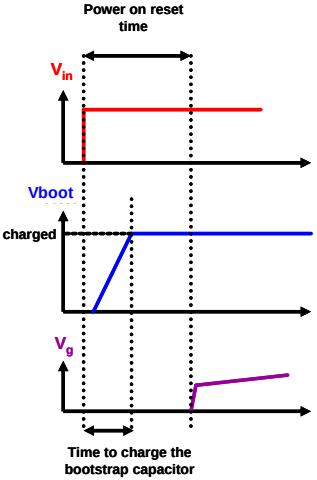
During the turn on and off phase, a high current (about a hundred mA) flows through the Vcc, the gnd and the boot. So the bootstrap capacitor and the decoupling must be as closer as possible. And it is forbidden to implement a resistor in series with the Gnd pin.

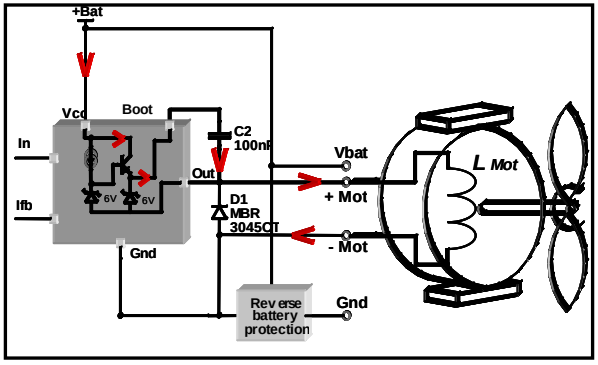


Bootstrap capacitor charge:

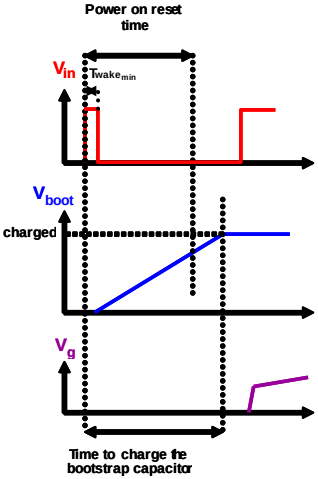
The power on reset is necessary to charge the bootstrap capacitor before turns on the power mosfet. The bootstrap capacitor gets its charge through the load. So the time to charge it depends of the load.

But the power on reset doesn't monitor the bootstrap capacitor voltage. Its time is set internally to allow starting the most of load without implement a special sequence:





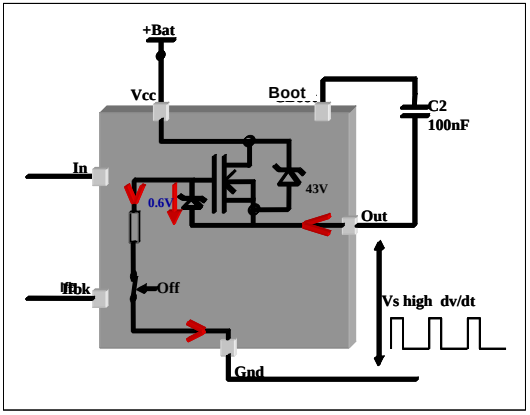
- If the inductance of the load is lower than 500µH, the power on reset is enough long to charge the bootstrap capacitor before turns on the power mosfet.



- If the inductance of the load is higher than 500µH, the power on reset is not enough long to charge completely the bootstrap capacitor before turns on the power mosfet. So the micro-processor need to implement a special sequence to start the device without activates the output power mosfet. The µp send one short pulse (Twake min < short pulse < Tpwr_on_rst) then wait for the bootstrap capacitor is totally charged and after provide the appropriate duty cycle.

The bootstrap charge depends of the battery voltage, the bootstrap capacitor value and the inductance load value.

Output high dv/dt immunity system:

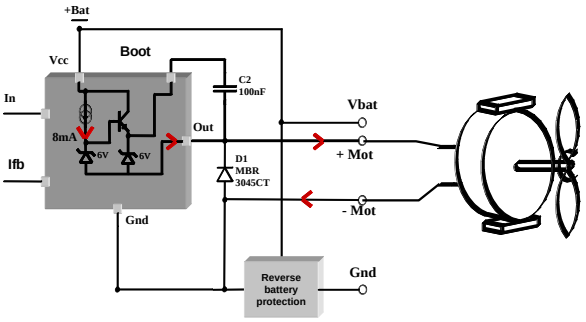


The IR3330S has a high dv/dt immunity system. This function creates a negative gate biasing if the output voltage exceed 1.7V. So this device can be implemented in an H-bridge configuration.

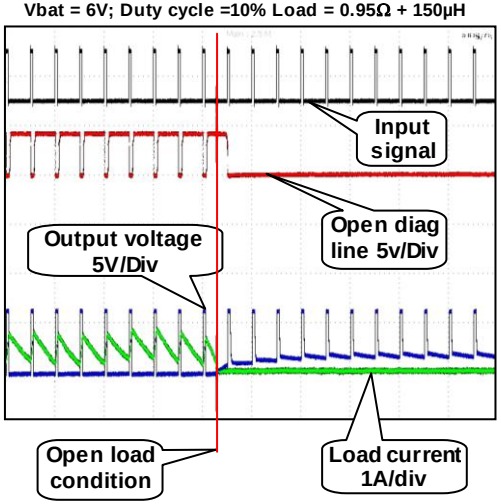
Open load detection function:

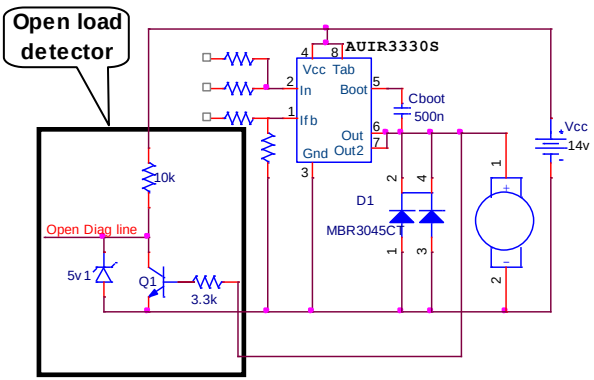
The bootstrap regulator bias provides a current on device output. If the impedance betw een the Output and ground is too high, after the turn off of the output mosfet, the output never reaches the ground. So it becomes possible to detect easily an open load condition w hen the device sw itches. In fully on condition the open load condition w ill detect by the current feedback (easy thanks to a high current condition).

In the schematic below the component R7, Q1, R8, D2 create the detection open load and provide a logic level diagnostic (open diag line) even if the battery in low voltage condition.



Vbat = 6V; Duty cycle =10% Load = 0.95Ω + 150µH





EMI consideration:

At vehicle level:

This is typical schematic of a high frequency power module in a vehicle (see: Figure 6: Typical schematic of a power module in a vehicle) with the parasitic element create by the connection wire. Between the battery and the module, the voltage is almost constant and the current switch at the application frequency. The power line creates a parasitic inductance with the current variation that generates voltage spike on the battery line. The level of this spike is directly linked to the conducted emissions level on the battery line. So control the current variation or the di/dt value reduces the conducted EMI level on the battery line. In this case use the AUIR3330 (active di/dt control) allows reducing significantly the conduced EMI level.
By analogy between the module and the load (see: Figure 6: Typical schematic of a power module in a vehicle), due to the high inductance value of the motor, the current is almost constant and the voltage switches at the application frequency. Due to the parasitic capacitor of the load each voltage variation create current spike on the load line. The level of this spike is directly linked to the radiated emissions level on the load line. So control the voltage variation or the dv/dt value reduces the radiated EMI level. In this case use the AUIR3340 (active dv/dt control) allows reducing significantly the radiated EMI level.

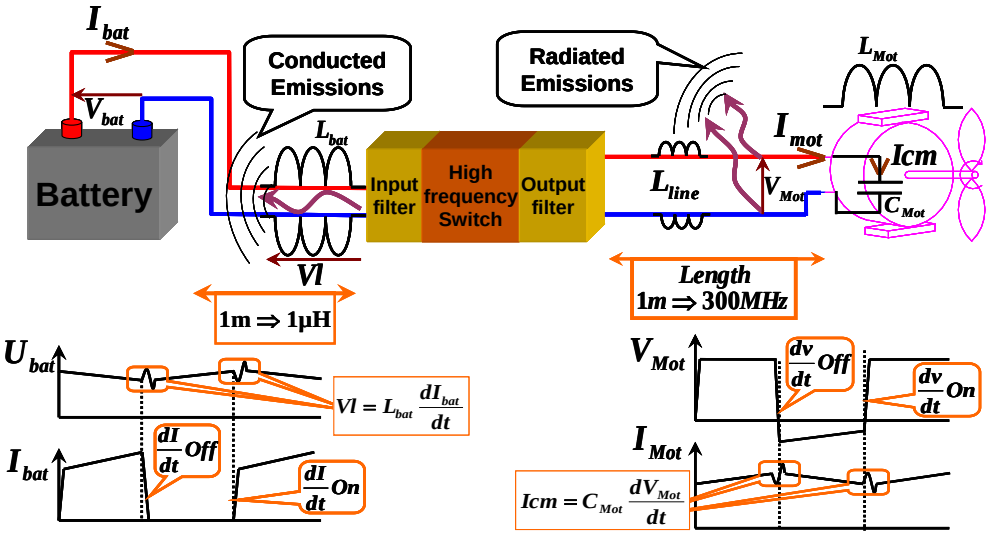


Figure 6: Typical schematic of a power module in a vehicle

At module level:

This typical schematic takes into account the parasitic elements created by the PCB tracks. Its impedance is $Ztrace = R + jL\omega$.

$\omega = 2\pi F$

Due to the $jL\omega$ element, the current variation in each line must be smooth to avoid the over voltage spikes.

$$U_l = L\frac{Di}{Dt}$$

The impedance value of the parasitic element Z3 and Z6 are negligible compare to the motor impedance. So they don't have an important influence on the EMI perturbation level.

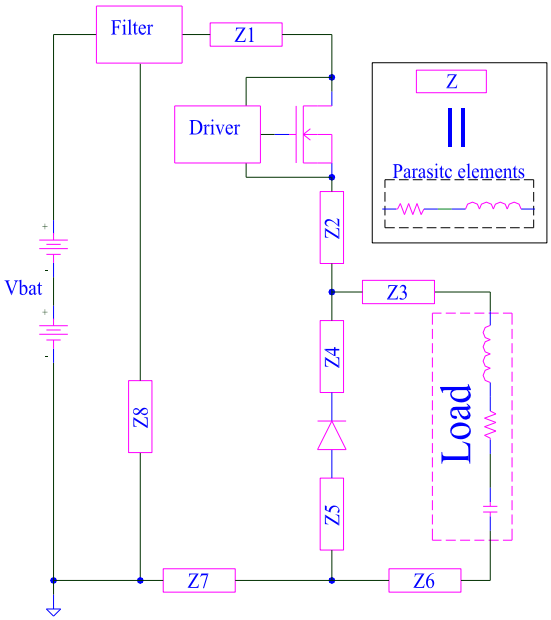


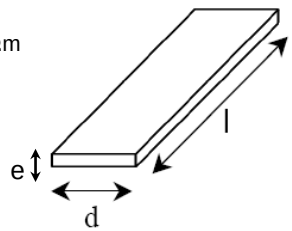
Figure 7: typical schematic of a power module

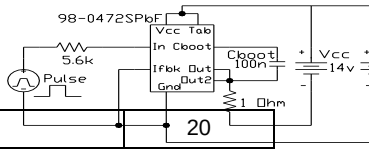
The parasitic component evaluation for DC and low frequency conditions are:

- $R = \rho\frac{l}{S}$
- $L = 0.2\times10^{-6}\times l\times\left[\ln(\frac{2\times l}{d+e}) + 0.5 + 0.22(\frac{d+e}{l})\right]$

Where:

- ρ : material resistivity Cu = 1.7x10^{-8}Ωm
- l : track length in m
- S : track section in m² (d x e)
- d : track width in m
- e : track thickness in m





Example:

If the copper track characteristic between the MOSFET pin and the free wheeling diode (parasitic element Z2) is:

- l = 2 cm
- d = 1mm
- e = 35µm

So

- R = 0.9mΩ
- L = 8nH

If the MOSFET switches without any slope control, the di/dt can reach 100A/µs. The overvoltage spike created by the current variation in the parasitic inductance is then

- U_l = 8n * (100/1E-6) = 800mv

Now , if the MOSFET slope is controlled and limited to 40A/µs. Then, the overvoltage spike created by the current variation in the parasitic inductance is:

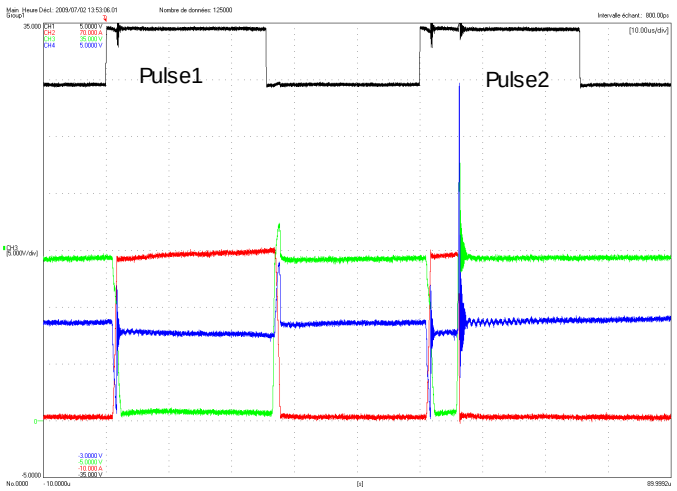
- U_l = 8n * (40/1E-6) = 320mV

Even if the PCB tracks are short, their parasitic impedances are not negligible in 20 kHz application. Limiting the current variation in these parasitic impedances reduces the overvoltage spikes so the noise level. For further information about the PCB impedance effect see the application note named “Using the AUIR3330/40: PCB layout recommendation” on the IR web site (www.irf.com).

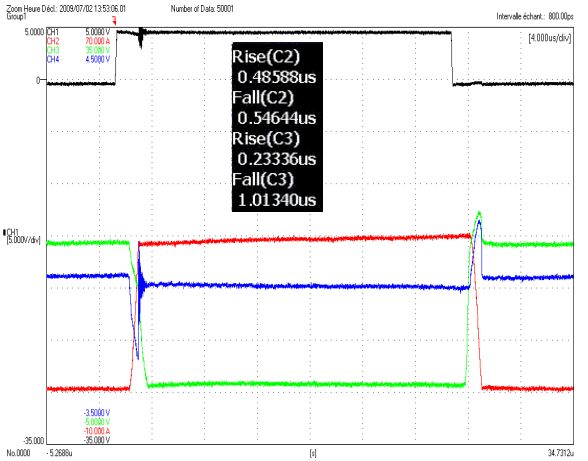
Measured impact of the di/dt control:

If the device detects an over current condition, it turns off the output MOSFET without di/dt sequence to reduce application stress. So a simple test, consists to look at the waveform before (pulse1) and during the over current protection shutdown (pulse 2) to see the di/dt impact with the same condition (even if the dv/dt stay constant).

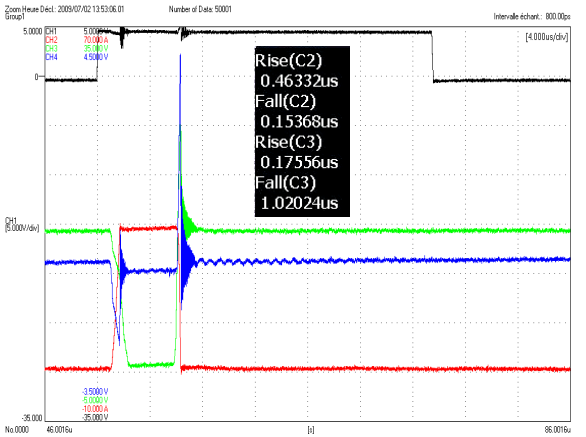
- Black (Ch1) = In_pwm 5V/div
- Red (Ch2) = drain current 10A/div
- Green (Ch3) = Vds (drain source voltage) 5V/div
- Blue (Ch4) = Vbat (battery voltage) in AC mode 1V/div



Pulse1) Oscilloscope screenshot in normal condition:
The perturbation on the Vbat line during the turn on is due to the discontinuity of the current in the diode and intensified by the current loop implemented between the input filter and the device to measure the drain current (di/dt).



2) Oscilloscope screenshot during the over current shutdown:
This screenshot is the next pulse after this one shows previously. The perturbation on the Vbat line during the turn on is due to the discontinuity of the current in the diode and intensified by the current loop implemented between the input filter and the device to measure the drain current (di/dt).



Remove the di/dt sequence only on the turn off increase strongly the perturbation level (more than 20dB) on the power line even if the output dv/dt value doesn't change.
Note that in this example, the di/dt on sequence is still activated. By analogy with the turn off, we can easily guessed that the over all noise level will be increase if we could only keep the dv/dt on and remove the di/dt on.

Parameters curves:

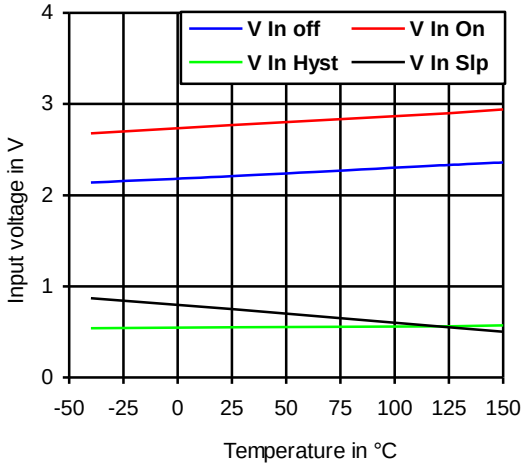


Figure 9: Input parameters vs. temperature

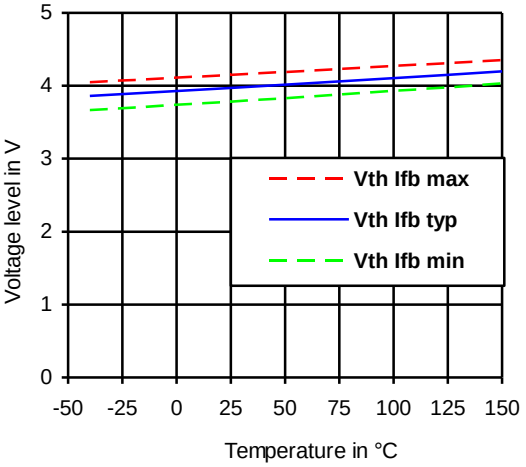


Figure 8: Vth Ifb vs. temperature

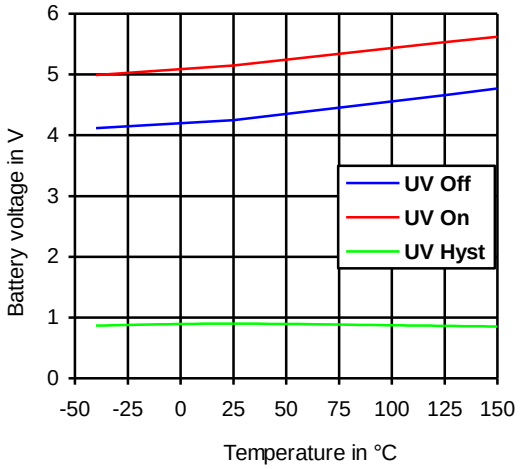


Figure 10: Under voltage parameters vs. temperature

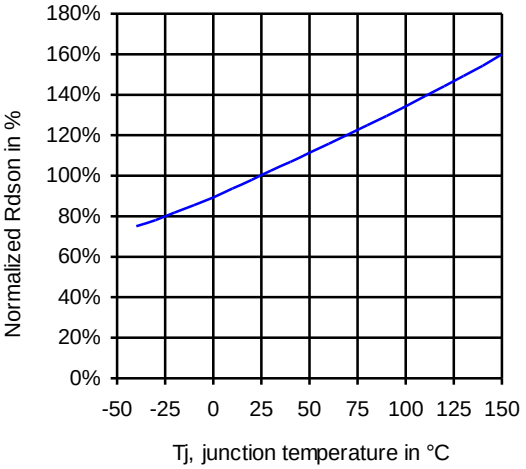


Figure 11: Normalized Rdson Vs Tj

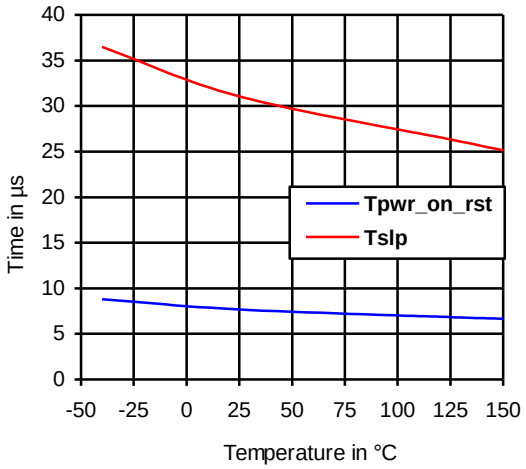


Figure 12: Tpwr_on_rst & Tslp vs. temperature

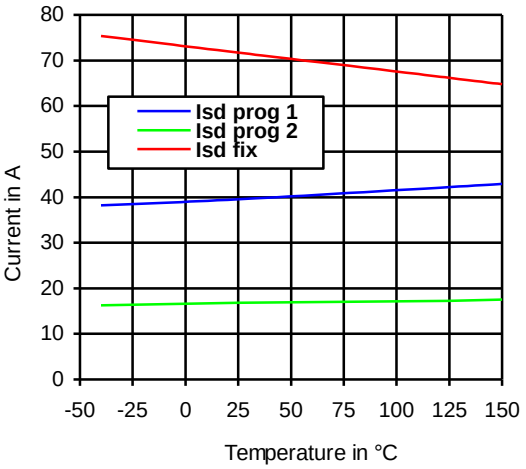


Figure 12: Current shutdown vs. temperature

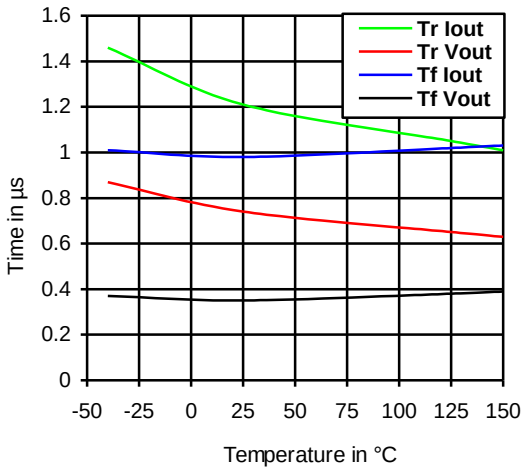


Figure 14: Rise and fall time vs. temperature

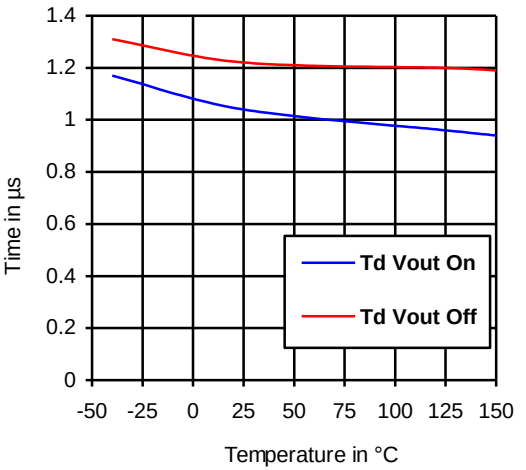


Figure 13: Tdon & off vs. temperature

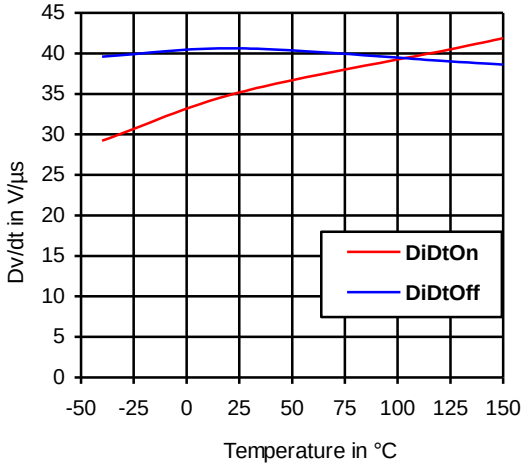


Figure 16: Dv/dt on & off vs. temperature

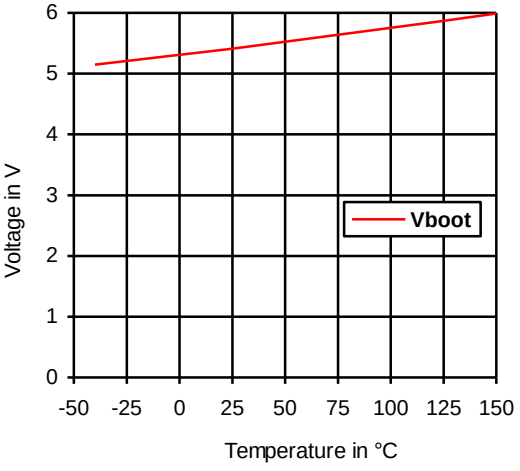


Figure 14: Bootstrap voltage vs. temperature

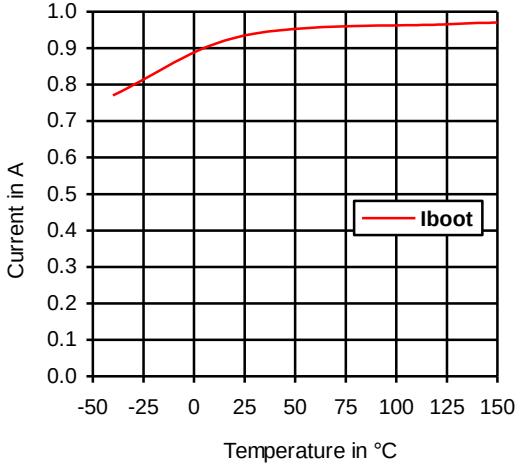


Figure 18: Current bootstrap vs. temperature

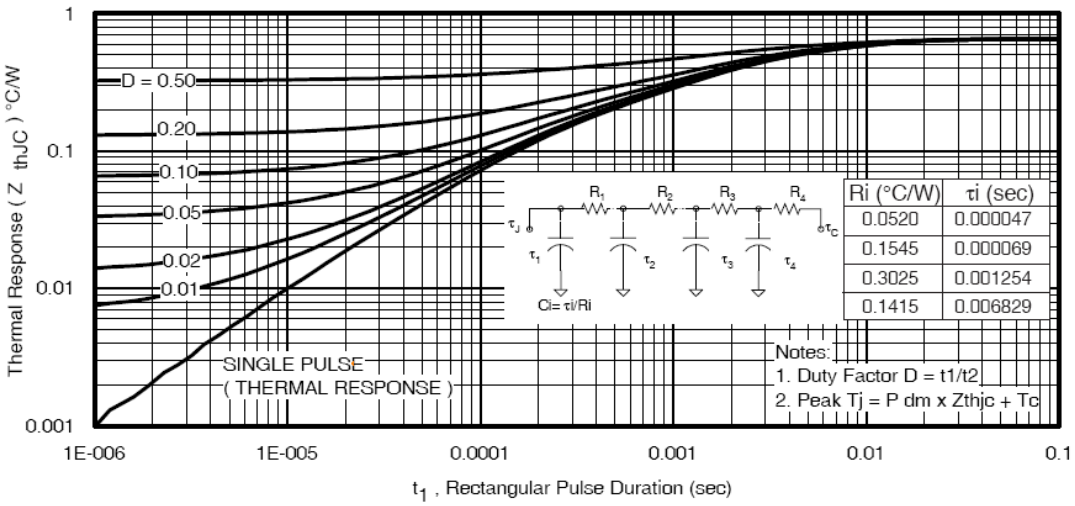
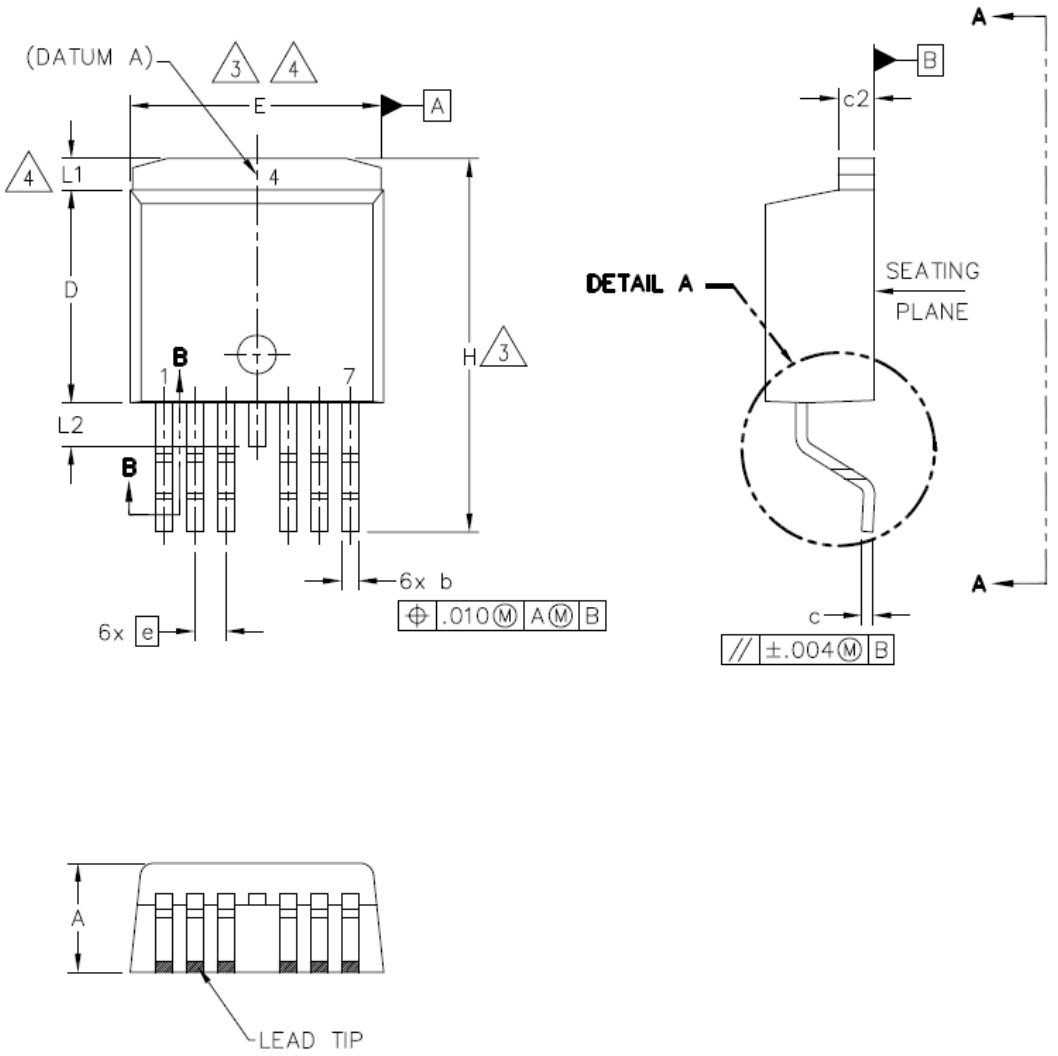


Figure 15: Transient thermal impedance and model vs. time

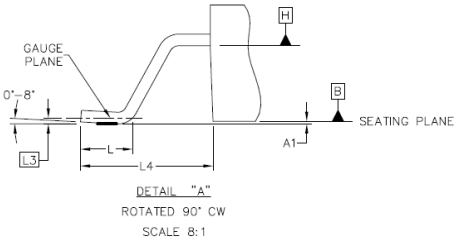
Case Outline 7L D2PAK



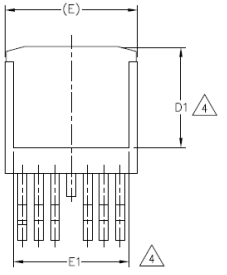
NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

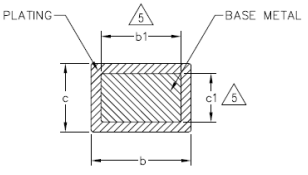
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	–	0.254	–	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	



DETAIL "A"
ROTATED 90° CW
SCALE 8:1

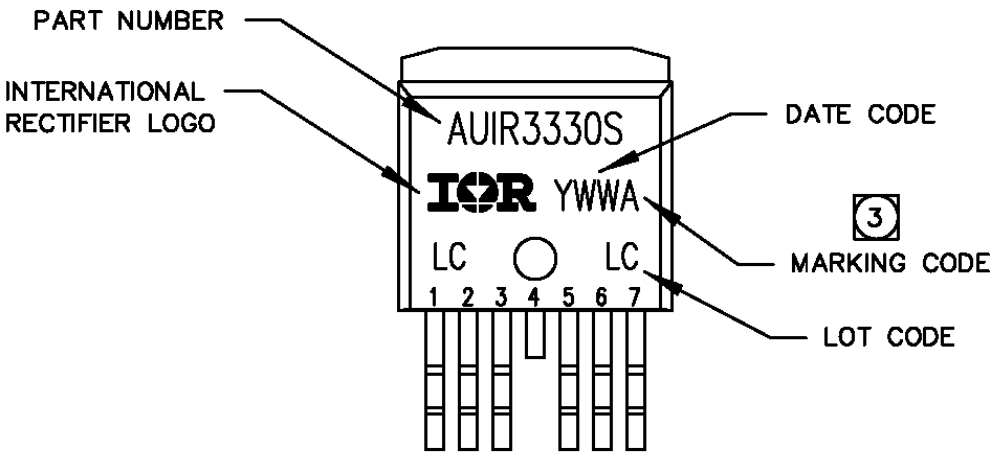


VIEW A–A



SECTION B–B
SCALE: NONE

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIR3330S	D2-Pak-7-Leads	Tube	50	AUIR3330S
		Tape and reel left	800	AUIR3330STRL
		Tape and reel right	800	AUIR3330STRR

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http://www.irf.com/technical-info/

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Tel: (310) 252-7105

Revision History

Revision	Date	Notes/Changes
A	29/01/10	First release
B	28-Jul-11	Update the MSL qualification level p2
C	15-Feb-12	Correct the ratio formula page 6