LDBL20

## 200 mA very low quiescent current linear regulator IC in (0.47x0.47) mm² STSTAMP™ package

Datasheet - production data

STSTAMP™ (0.47x0.47) mm²

- Internal constant current and thermal protections
- Available in STSTAMP™ (0.47x0.47) mm² package
- Operating temperature range: -40 °C to 125 °C

Application

- Mobile phones
- Tablet
- Digital still cameras (DSC)
- Wearable devices
- Portable media players

Description

The LDBL20 high accuracy voltage regulator provides 200 mA of maximum current from an input voltage ranging from 1.5 V to 5.5 V, with a typical dropout voltage of 200 mV.

It is available in the new STSTAMP™ package, allowing the maximum space saving.

The device is stabilized with a ceramic capacitor on the output. The ultra low drop voltage, low quiescent current and low noise features, together with the internal soft-start circuit, make the LDBL20 suitable for low power battery-operated applications.

An enable logic control function puts the LDBL20 in shutdown mode with a total current consumption lower than 0.2 µA. Constant current and thermal protection are provided.

Features

- Input voltage from 1.5 to 5.5 V
- Ultra low-dropout voltage (200 mV typ. at 200 mA load)
- Very low quiescent current (20 µA typ. at no-load, 0.03 µA typ. in off mode)
- Output voltage tolerance: ± 1.5% @ 25 °C
- 200 mA guaranteed output current
- High PSRR (80 dB@1 kHz, 50 db@100 kHz)
- Wide range of output voltages available on request: from 0.8 V up to 5.0 V in 50 mV step
- Logic-controlled electronic shutdown
- Internal soft-start
- Optional output voltage discharge feature
- Compatible with ceramic capacitor C_{OUT} = 0.47 µF

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Contents

1   Diagram

Figure 1: Block diagram

AM13852V1
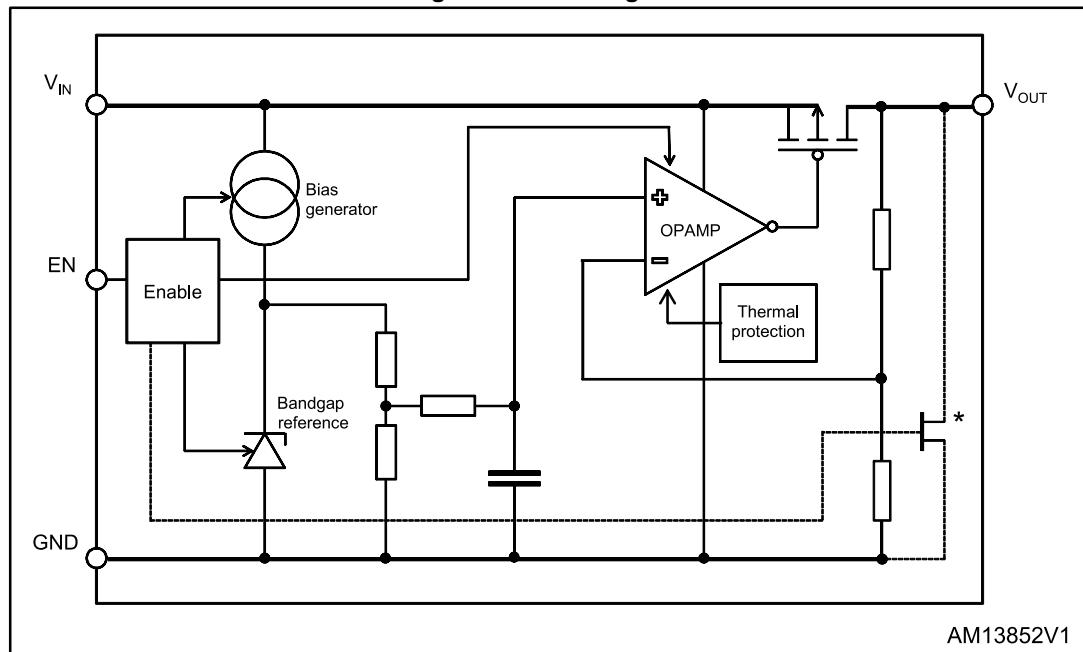
> The output discharge MOSFET is optional.

2 Pin configuration

Figure 2: Pin connection

GIPD310820151050MT
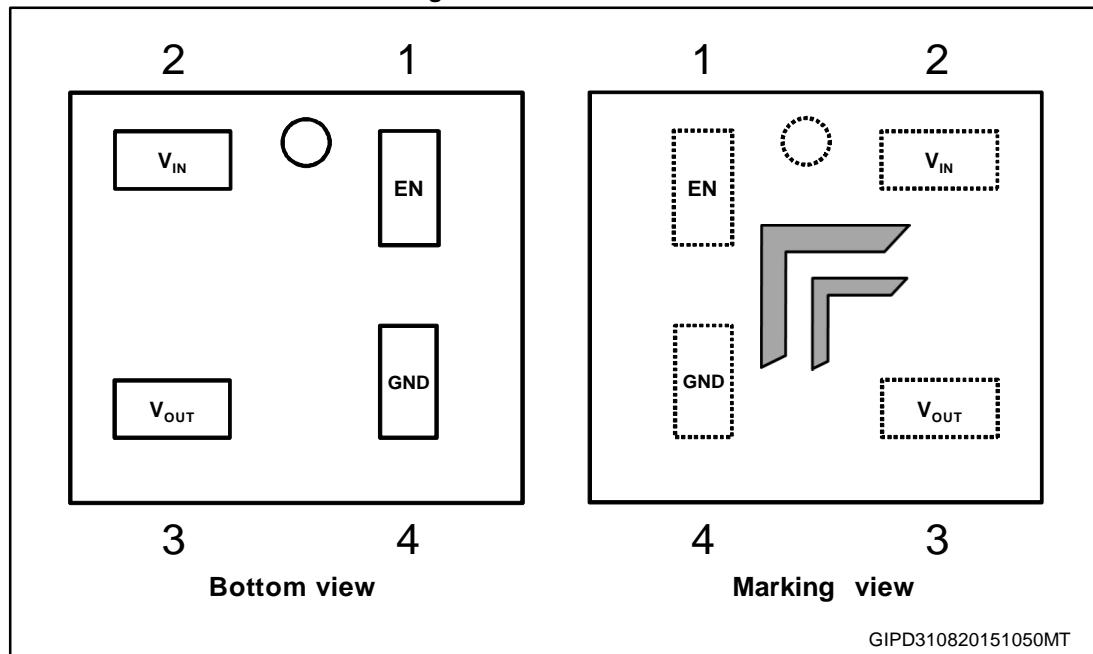
Table 1: Pin description

Pin	Symbol	Function
3	OUT	Output voltage
4	GND	Common ground
1	EN	Enable pin logic input: low = shutdown, high = active
2	IN	Input voltage

3 Typical application

Figure 3: Typical application circuits

GIPD310820151119MT
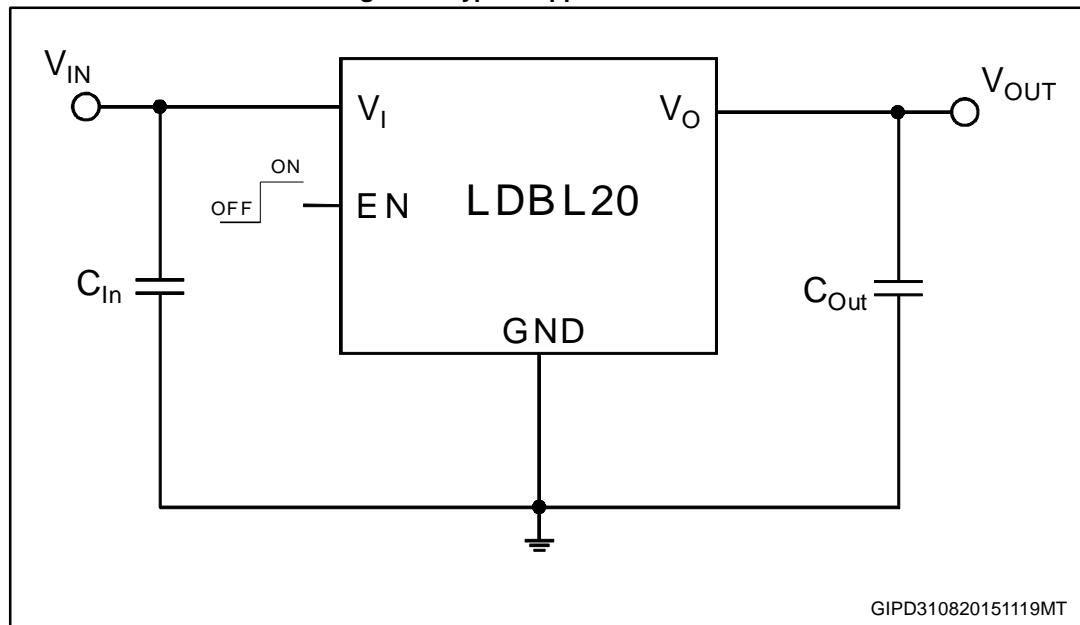
4   Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	- 0.3 to 7	V
V_{OUT}	Output voltage	- 0.3 to V_{IN} + 0.3	V
V_{EN}	Enable input voltage	- 0.3 to 7	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 40 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

> Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 3: ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	4	kV
		MM	400	V
		CDM	500	V

5   Electrical characteristics

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V or 1.5 V, whichever is greater, C_{IN} = C_{OUT} = 1 µF, I_{OUT} = 1 mA, V_{EN} = V_{IN}, unless otherwise specified.

Table 4: LDBL20 electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1.5		5.5	V
V_{OUT}	V_{OUT} accuracy	I_{OUT} = 1 mA, T_J = 25 °C	-1.5		+1.5	%
		I_{OUT} = 1 mA, -40 °C<T_J<125 °C	-3		+3	%
ΔV_{OUT}	Static line regulation[1]	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		0.02		%/V
		-40 °C<T_J<125 °C			0.2	
ΔV_{OUT}	Static load regulation	I_{OUT} = 0 mA to 200 mA		10		mV
		-40 °C<T_J<125 °C			0.01	%/mA
V_{DROP}	Dropout voltage	I_{OUT} = 30 mA, V_{OUT} = 2.8 V		35		mV
		I_{OUT} = 200 mA, V_{OUT} = 2.8 V, -40 °C<T_J<125 °C		200	350	
e_N	Output noise voltage	10 Hz to 100 kHz, I_{OUT} = 10 mA		45		µV_{RMS}
SVR	Supply voltage rejection	V_{IN} = $V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V Frequency =1 kHz I_{OUT} = 30 mA		80		dB
		V_{IN} = $V_{OUT(NOM)}$+ 1 V +/- V_{RIPPLE} V_{RIPPLE} = 0.2 V Frequency = 100 kHz I_{OUT} = 30 mA		55		
I_Q	Quiescent current	I_{OUT} = 0 mA		20	40	µA
		I_{OUT} = 200 mA		100		
$I_{Standby}$	Standby current	V_{IN} input current in OFF mode: V_{EN} = GND		0.03	0.2	µA
I_{SC}	Short-circuit current	R_L = 0	250	350		mA
R_{ON}	Output voltage discharge MOSFET	(LD39020DT only)		100		Ω
V_{EN}	Enable input logic low	V_{IN} = 1.5 V to 5.5 V -40 °C<T_J<125 °C			0.4	V
	Enable input logic high	V_{IN} = 1.5 V to 5.5 V -40 °C<T_J<125 °C	1			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}			100	nA
T_{ON}[2]	Turn-on time			100		µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{SHDN}	Thermal shutdown			160		°C
	Hysteresis			20		
C_{OUT}	Output capacitor	Capacitance	0.47		22	µF

Notes:

[1]Not applicable for Vout(nom) > 4.5 V

[2]Turn-on time is time measured between the enable input just exceeding VEN high value and the output voltage just reaching 95 % of its nominal value

6 Application information

6.1 Soft-start function

The LDBL20 has an internal soft-start circuit. By increasing the startup time up to 100 μs, without the need of any external soft-start capacitor, this feature keeps the regulator inrush current at startup under control.

6.2 Output discharge function

The LDBL20 integrates a MOSFET connected between V_{OUT} and GND. This transistor is activated when the EN pin goes to low logic level and has the function to quickly discharge the output capacitor when the device is disabled by the user.

The device is available with or without the auto-discharge feature. See *Table 6: "Order code"*.

6.3 Input output capacitors

The LDBL20 requires external capacitors to assure the regulator control loop stability.

Any good quality ceramic capacitor can be used but, the X5R and the X7R are suggested since they guarantee a very stable combination of capacitance and ESR overtemperature.

Locating the input/output capacitors as closer as possible to the relative pins is recommended.

The LDBL20 requires an input capacitor with a minimum value of 1 μF.

This capacitor must be located as closer as possible to the input pin of the device and returned to a clean analog ground.

The control loop of the LDBL20 is designed to work with an output ceramic capacitor.

This capacitor must meet the requirements of minimum capacitance and equivalent series resistance (ESR), as shown in *Figure 17: "Stability area vs (COUT, ESR)"*. To assure stability, the output capacitor must maintain its ESR and capacitance in the stable region, over the full operating temperature range.

The LDBL20 shows stability with a minimum effective output capacitance of 220 nF.

However, to keep stability in all operating conditions (temperature, input voltage and load variations), a minimum output capacitor of 0.47 μF is recommended.

The suggested combination of 1 μF input and output capacitors offers a good compromise among the stability of the regulator, optimum transient response and total PCB area occupation.

7 Typical characteristics

(C_{IN} = C_{OUT} = 1 μF, V_{EN} to V_{IN}, T_J = 25 °C unless otherwise specified)

Figure 4: Output voltage vs temperature (I_{OUT} = 1 mA)

V_{IN} = 4.3 V, I_{OUT} = 1 mA

AM13855V1
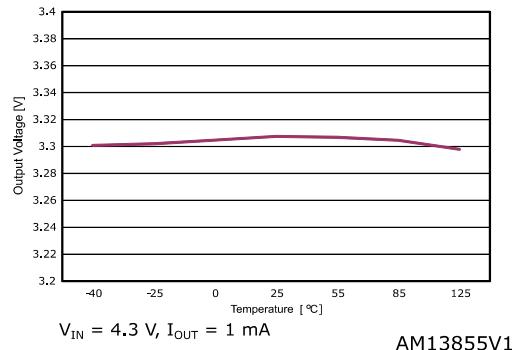
Figure 5: Output voltage vs temperature (I_{OUT} = 200 mA)

V_{IN}=4.3V, I_{OUT}=200mA

AM13856V1
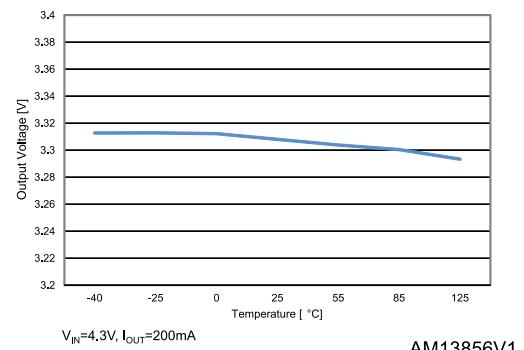
Figure 6: Line regulation vs temperature

V_{IN} = 4.3 V to 5.5 V, I_{OUT} = 10 mA

AM13857V1
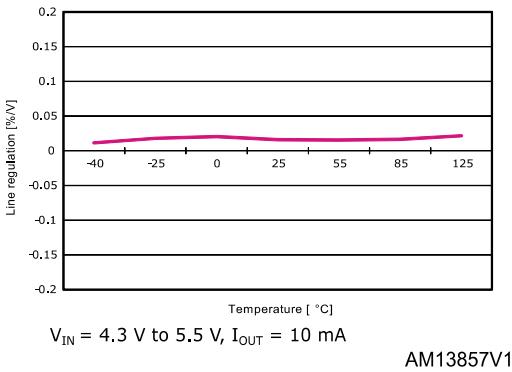
Figure 7: Load regulation vs temperature

V_{IN}=4.3V, I_{OUT}= 0 to 200mA

AM13858V1
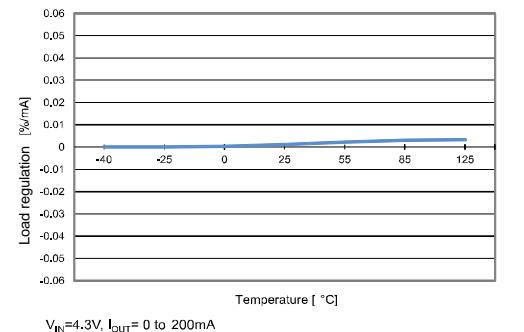
Figure 8: Quiescent current vs temperature (I_{OUT} = 0 mA)

V_{IN} = 4.3 V, I_{OUT} = 0 mA

AM13859V1
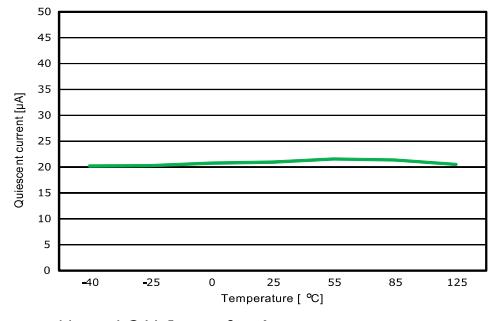
Figure 9: Quiescent current vs temperature (I_{OUT} = 200 mA)

V_{IN}=4.3V, I_{OUT}= 200mA

AM13860V1
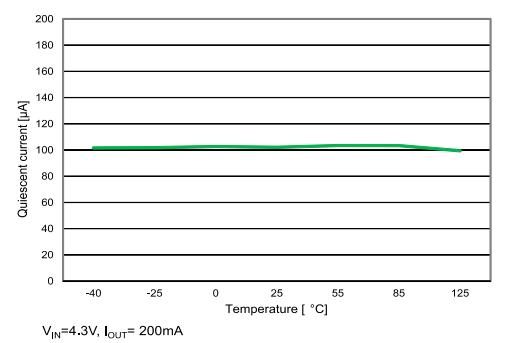
Figure 10: Shutdown current vs temperature

V_{IN} = V, V_{EN} = GND

AM13861V1
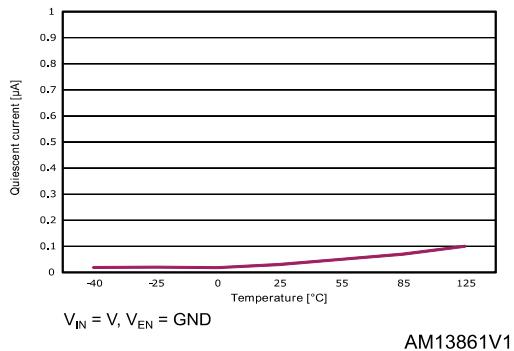
Figure 11: Quiescent current vs load current

V_{IN}=2V, V_{OUT}=1V

AM13862V1
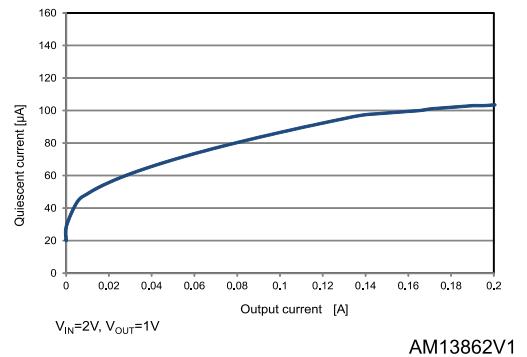
Figure 12: Quiescent current vs input voltage

V_{IN} = 2 V, V_{OUT} = 1 V

AM13863V1
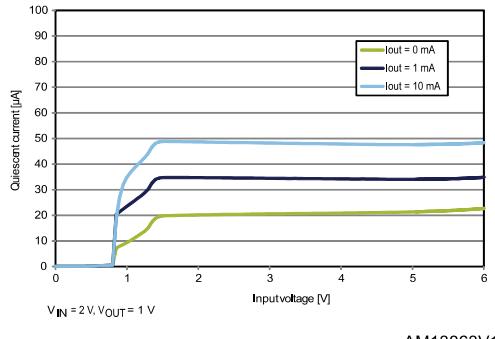
Figure 13: Dropout voltage vs temperature

AM13864V1
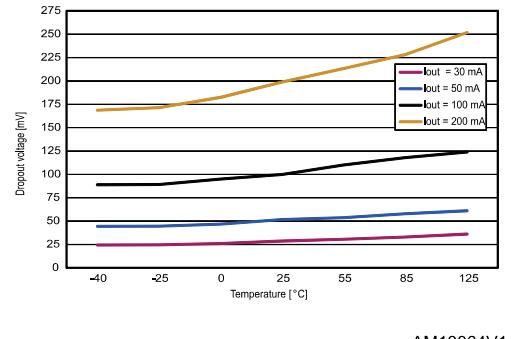
Figure 14: Supply voltage rejection vs frequency

V_{IN} 2 V +/- 200 m V, V_{OUT} = 1 V, C_{OUT} = 1 μF

AM13865V1
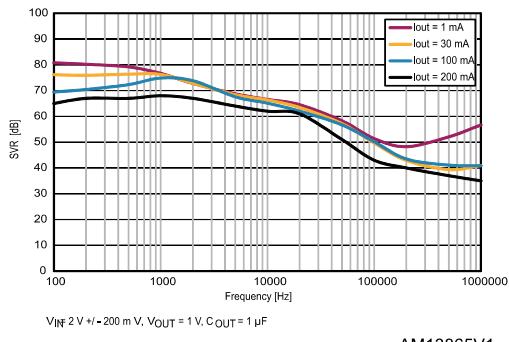
Figure 15: Supply voltage rejection vs input voltage

I_{OUT} = 30mA, V_{OUT} = 1 V, C_{OUT} = 1 μF

AM13866V1
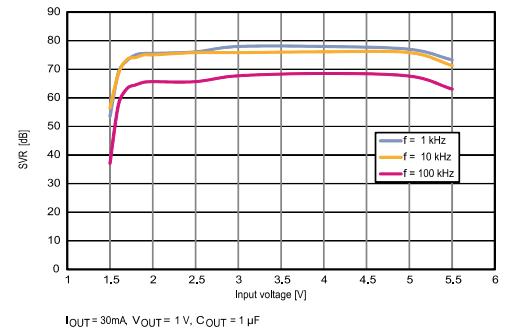
Figure 16: Output noise spectral density

$V_{IN} = 2.0$ V, $V_{OUT} = 1.0$ V, $C_{IN} = C_{OUT} = 1$ µF

AM13867V1

Figure 17: Stability area vs (C_{OUT}, ESR)

STABILITY AREA

V_{IN} from 2 to 5.5 V, I_{OUT} from 0 to 300 mA, $C_{IN} = 1$ µF

AM13868V1
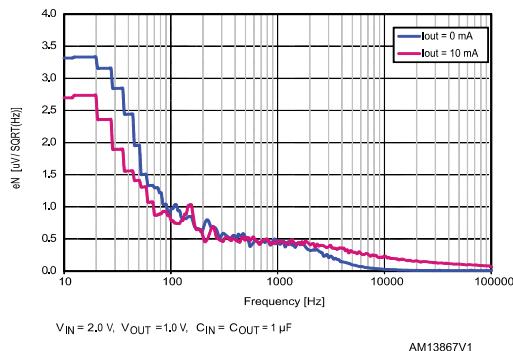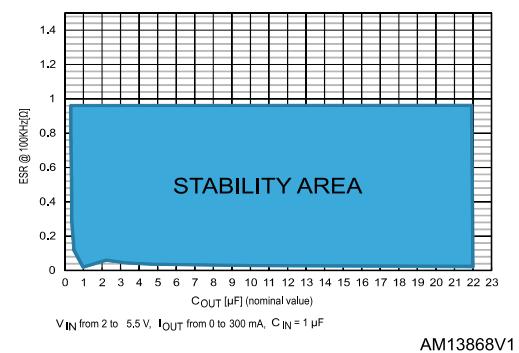
Figure 18: Enable startup ($V_{OUT} = 1$ V)

V_{EN}

V_{OUT}

I_{OUT}

$V_{IN} = 2$ V, $V_{EN} = 0$ V to V_{IN}, $I_{OUT} = 0.2$ A, $V_{OUT} = 1$ V, $T_r = 5$ µs

AM13869V1
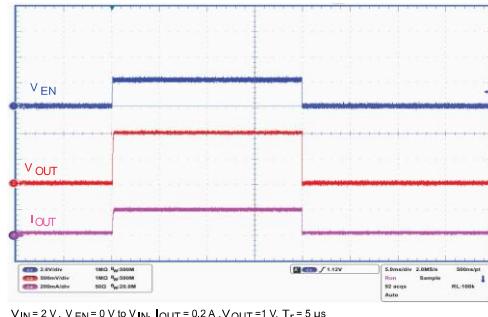
Figure 19: Enable startup ($V_{OUT} = 5$ V)

V_{EN}

V_{OUT}

I_{OUT}

$V_{IN} = 5.5$ V, $V_{EN} = 0$ V to 2 V, $I_{OUT} = 0.2$A, $V_{OUT} = 5$ V, $T_r = 5$ µs

AM13870V1
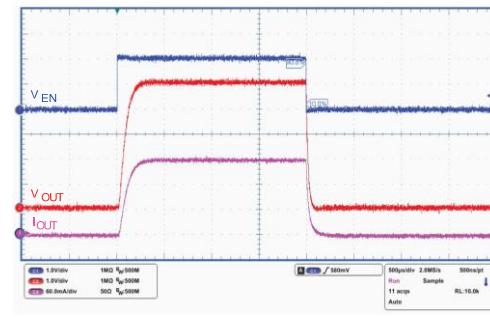
Figure 20: Turn-on time ($V_{OUT} = 1$ V)

V_{IN}

V_{OUT}

I_{OUT}

$V_{IN} = V_{EN} =$ from 0 V to 5.5 V, $I_{OUT} = 0.2$ A, $V_{OUT} = 1$ V, $T_r = 5$ µs

AM13871V1
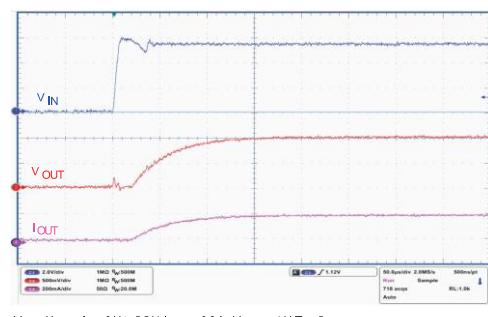
Figure 21: Turn-off time ($V_{OUT} = 1$ V)

V_{IN}

V_{OUT}

I_{OUT}

$V_{IN} = V_{EN} =$ from 5.5 V to 0 V, $I_{OUT} = 0.2$ A, $V_{OUT} = 1$ V, $T_f = 5$ µs

AM13872V1
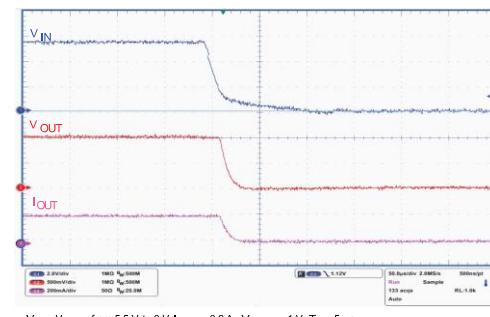
Figure 22: Turn-on time (V$_{OUT}$ = 5 V)
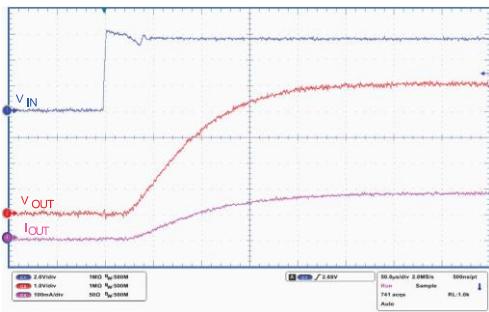
V$_{IN}$ = V$_{EN}$ = from 0 V to 5.5 V, I$_{OUT}$ = 0.2 A, V$_{OUT}$ = 5 V, T$_r$ = 5 μs

AM13873V1

Figure 23: Turn-off time (V$_{OUT}$ = 5 V)
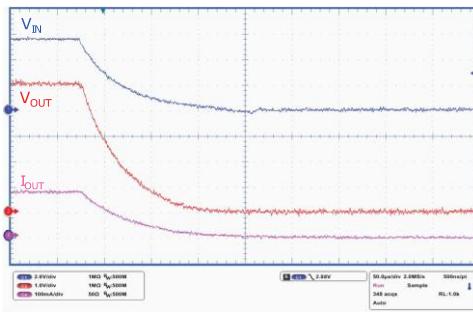
V$_{IN}$ = V$_{EN}$ = from 5.5 V to 0 V, I$_{OUT}$ = 0.2 A, V$_{OUT}$ = 5 V, T$_f$ = 5 μs

AM13874V1

Figure 24: Line transient (V$_{OUT}$ = 1 V)
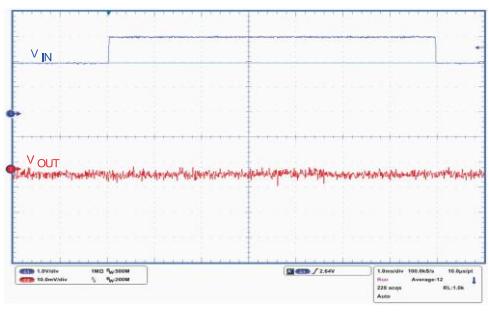
V$_{IN}$ = V$_{EN}$ = from 2 V to 3 V , I$_{OUT}$ = 10 mA , V$_{OUT}$ = 1 V, T$_r$ = T$_f$ = 5 μs

AM13875V1

Figure 25: Line transient (V$_{OUT}$ = 5 V)
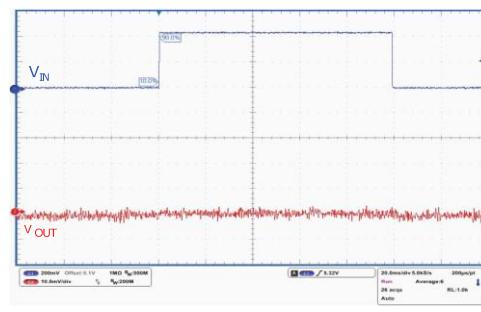
V$_{IN}$ = V$_{EN}$ = from 5.1 V to 5.5 V, I$_{OUT}$ = 10 mA , V$_{OUT}$ = 5 V, T$_r$ = T$_f$ = 5 μs

AM13876V1

Figure 26: Load transient (V$_{OUT}$ = 1 V)
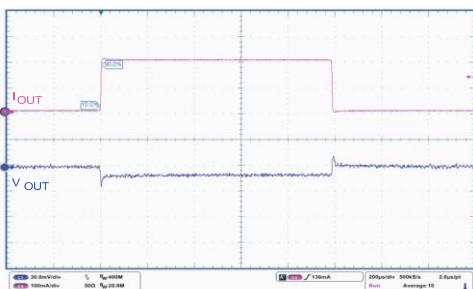
V$_{IN}$ = V$_{EN}$ = 2 V, I$_{OUT}$ = from 0 to 0.2 A, V$_{OUT}$ = 1 V, t$_r$ = t$_f$ = 5 μs

AM13877V1

Figure 27: Load transient (V$_{OUT}$ = 5 V)
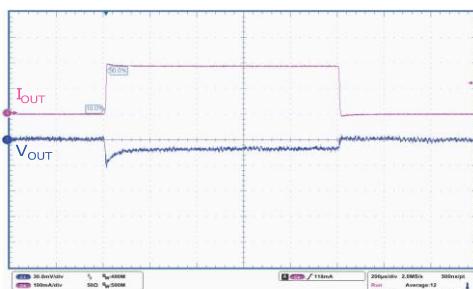
V$_{IN}$ = V$_{EN}$ = 5.5 V, I$_{OUT}$ = from 0 to 0.2 A , V$_{OUT}$ = 5 V, t$_r$ = t$_f$ = 5 μs

AM13878V1

8   Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1   STSTAMP™ (0.47x0.47) mm² package information

Figure 28: STSTAMP™ (0.47x0.47) mm² package outline

8351431_D
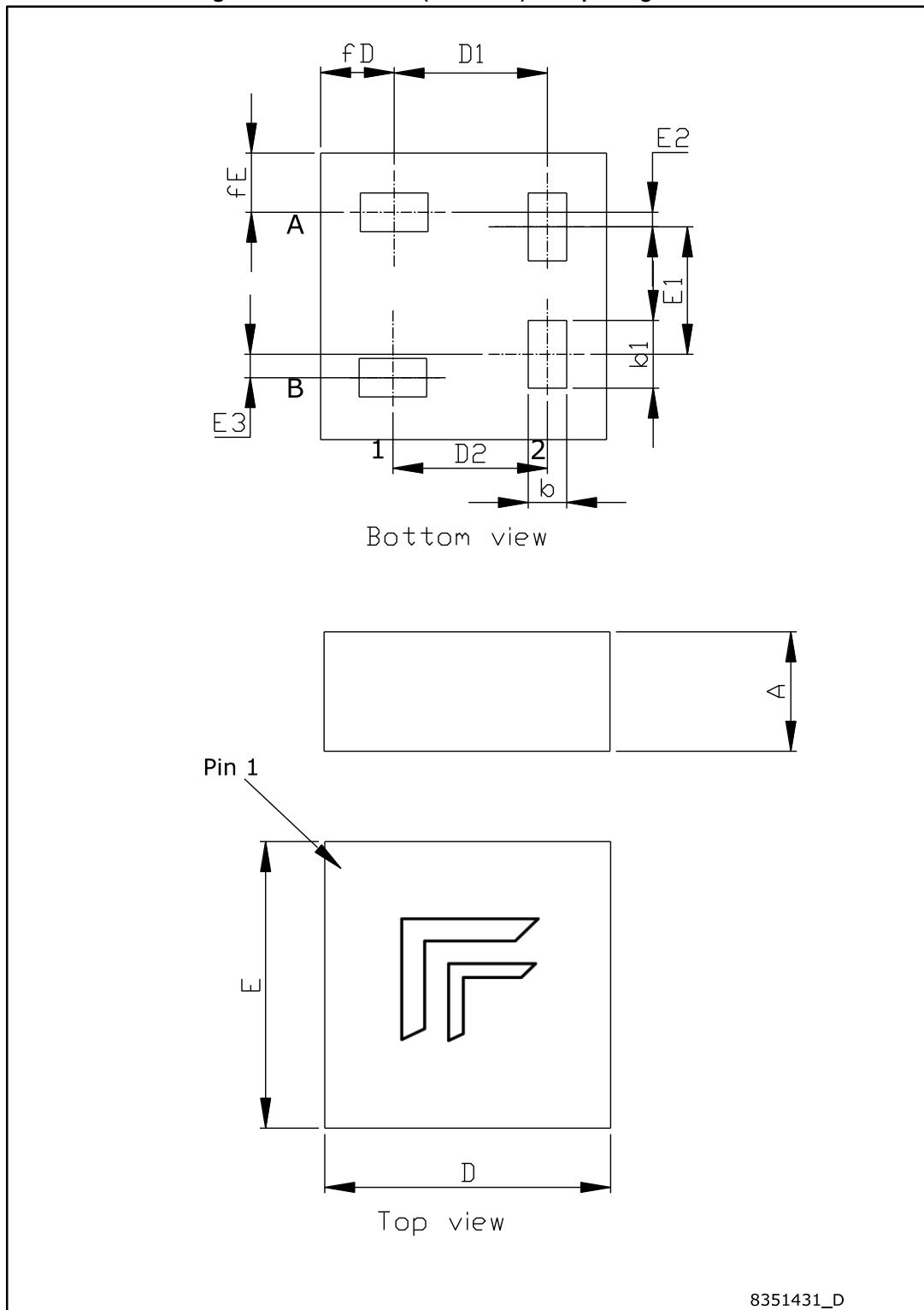
Table 5: STSTAMP™ (0.47x0.47) mm² mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	0.18	0.200	0.220
b	0.060	0.065	0.070
b1	0.109	0.114	0.119
E	0.450	0.480	0.510
E1	0.208	0.213	0.218
E2	0.019	0.024	0.029
E3	0.034	0.039	0.044
D	0.450	0.480	0.510
D1	0.252	0.257	0.262
D2	0.255	0.260	0.265
fE	0.095	0.101	0.106
fD	0.106	0.111	0.116

Figure 29: STSTAMP™ (0.47x0.47) mm² recommended footprint
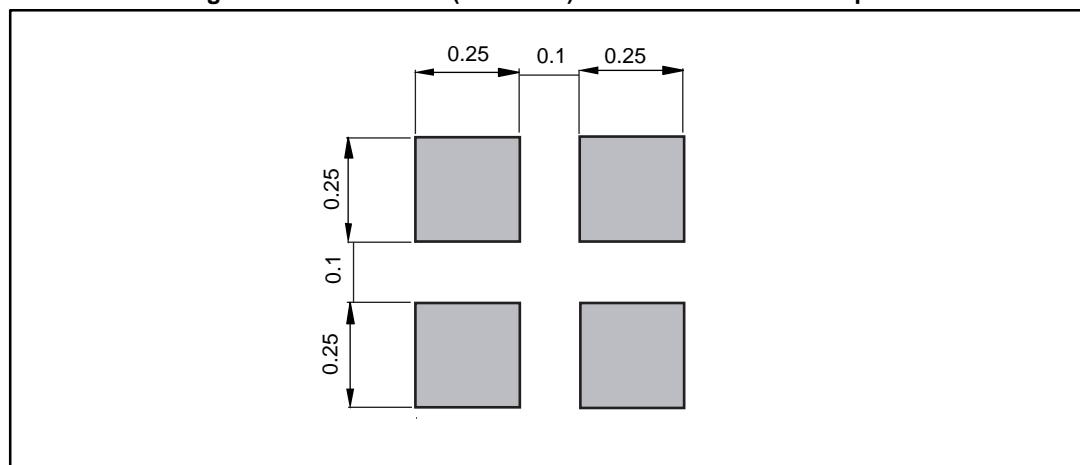
Figure 30: STSTAMP™ (0.47x0.47) mm² recommended solder stencil
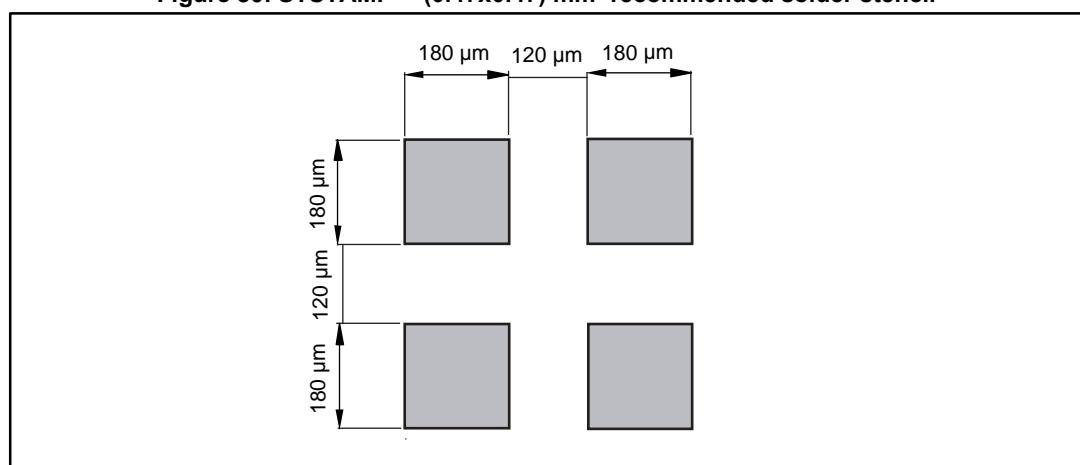
9   Ordering information

Table 6: Order code

Order code	Output voltage (V)	Auto-discharge	Packing
LDBL20D-xyR	x.y	Yes	Tape and reel

10 Revision history

Table 7: Document revision history

Date	Revision	Changes
10-Nov-2015	1	Initial release

IMPORTANT NOTICE – PLEASE READ CAREFULLY